

System Block Diagram

SYNC\_MASTER=(MASTER)SYNC\_DATE=(MASTER)

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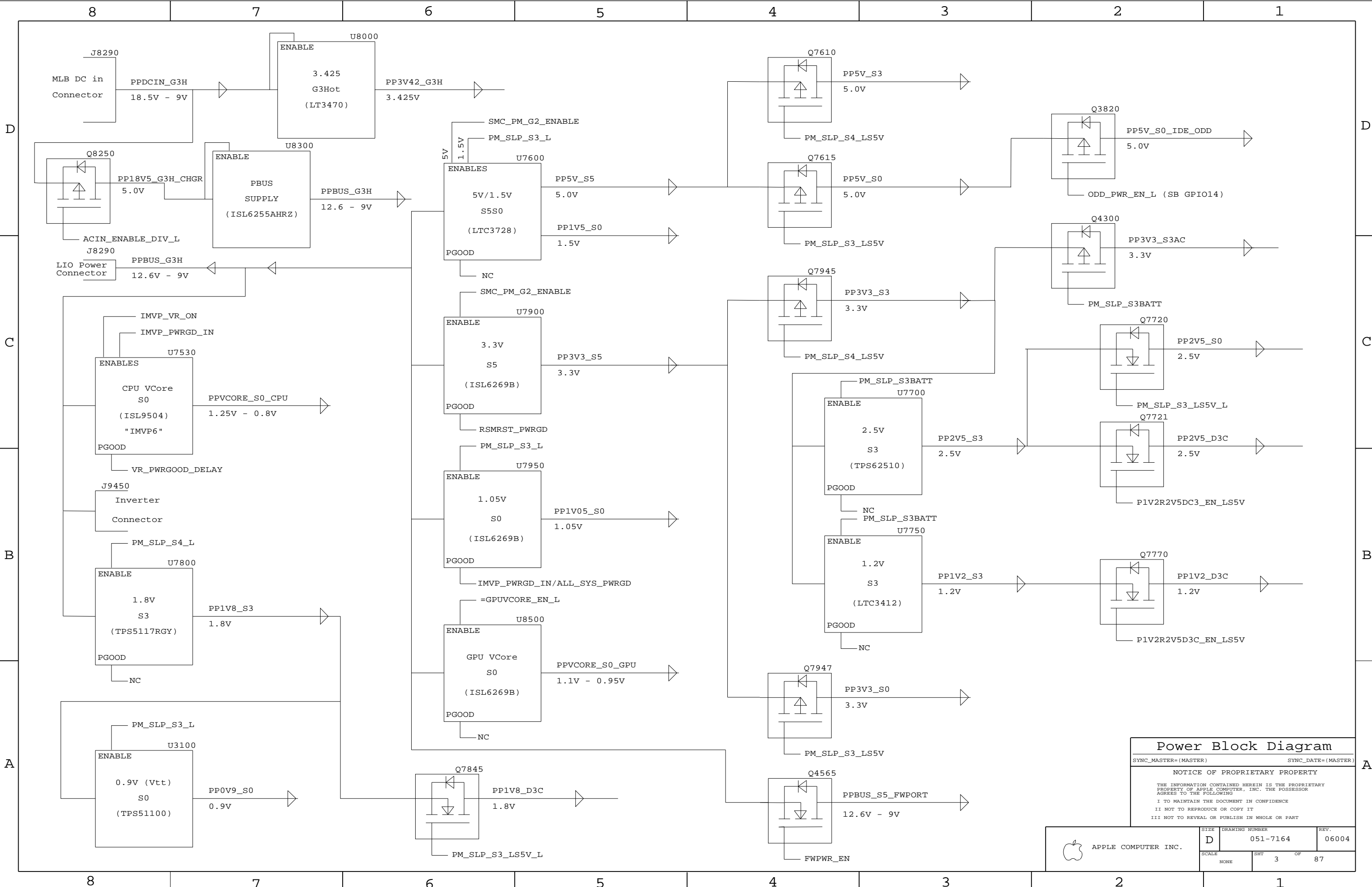
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 06004
	SCALE NONE	SHT 2	OF 87



Power Block Diagram

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SYNC\_DATE=(MASTER)

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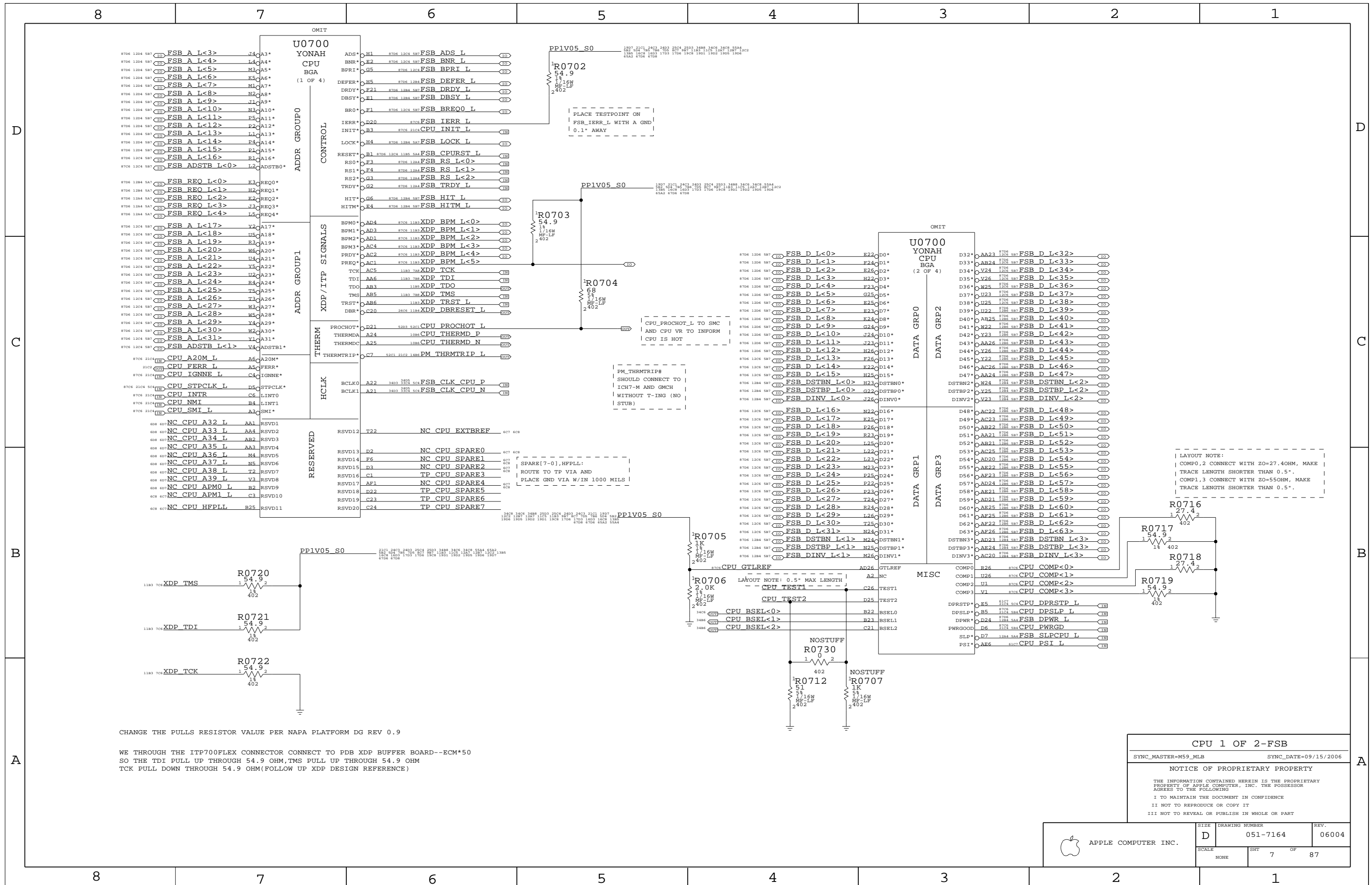
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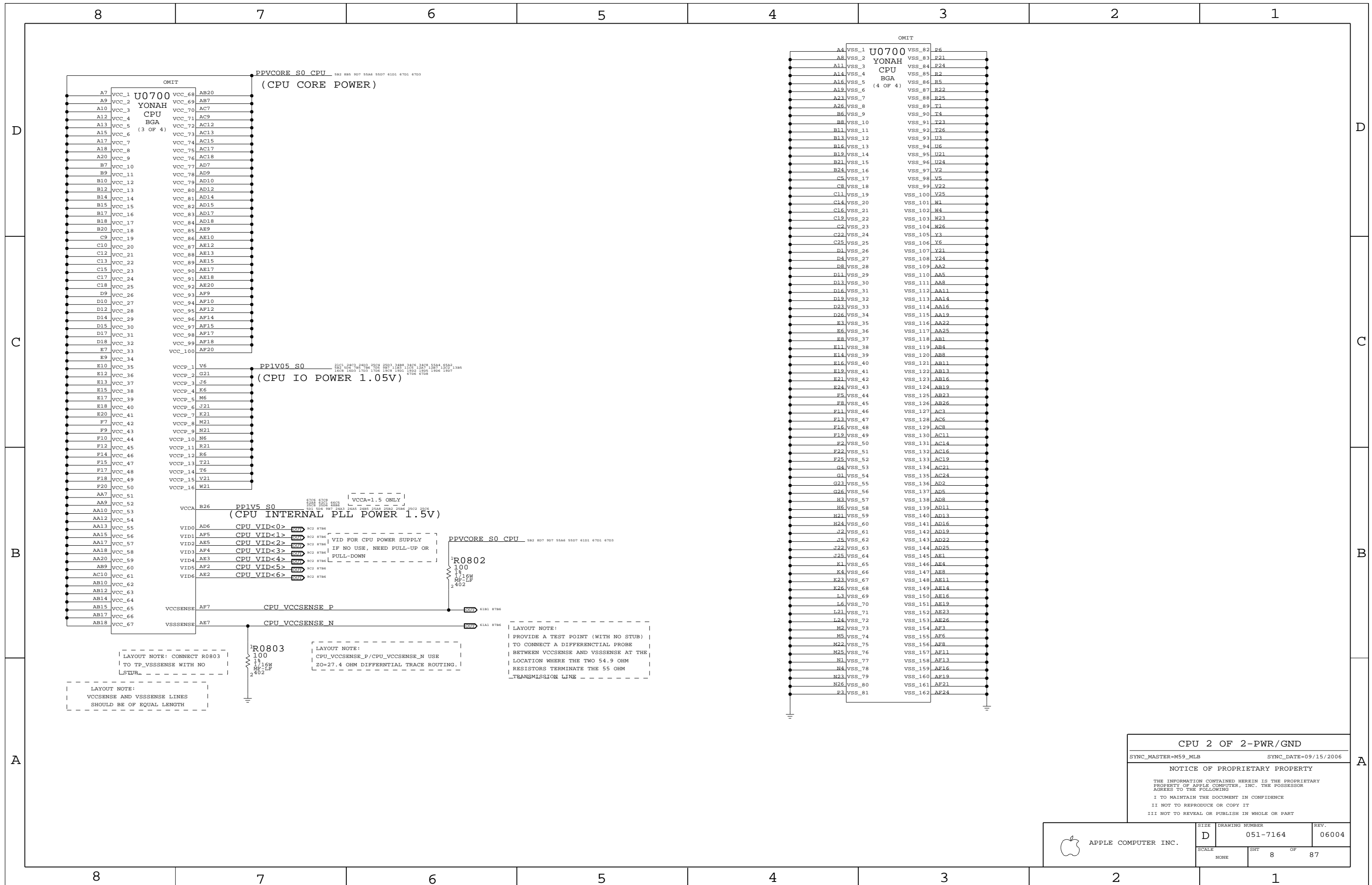
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE		SHT	OF
NONE		3	87

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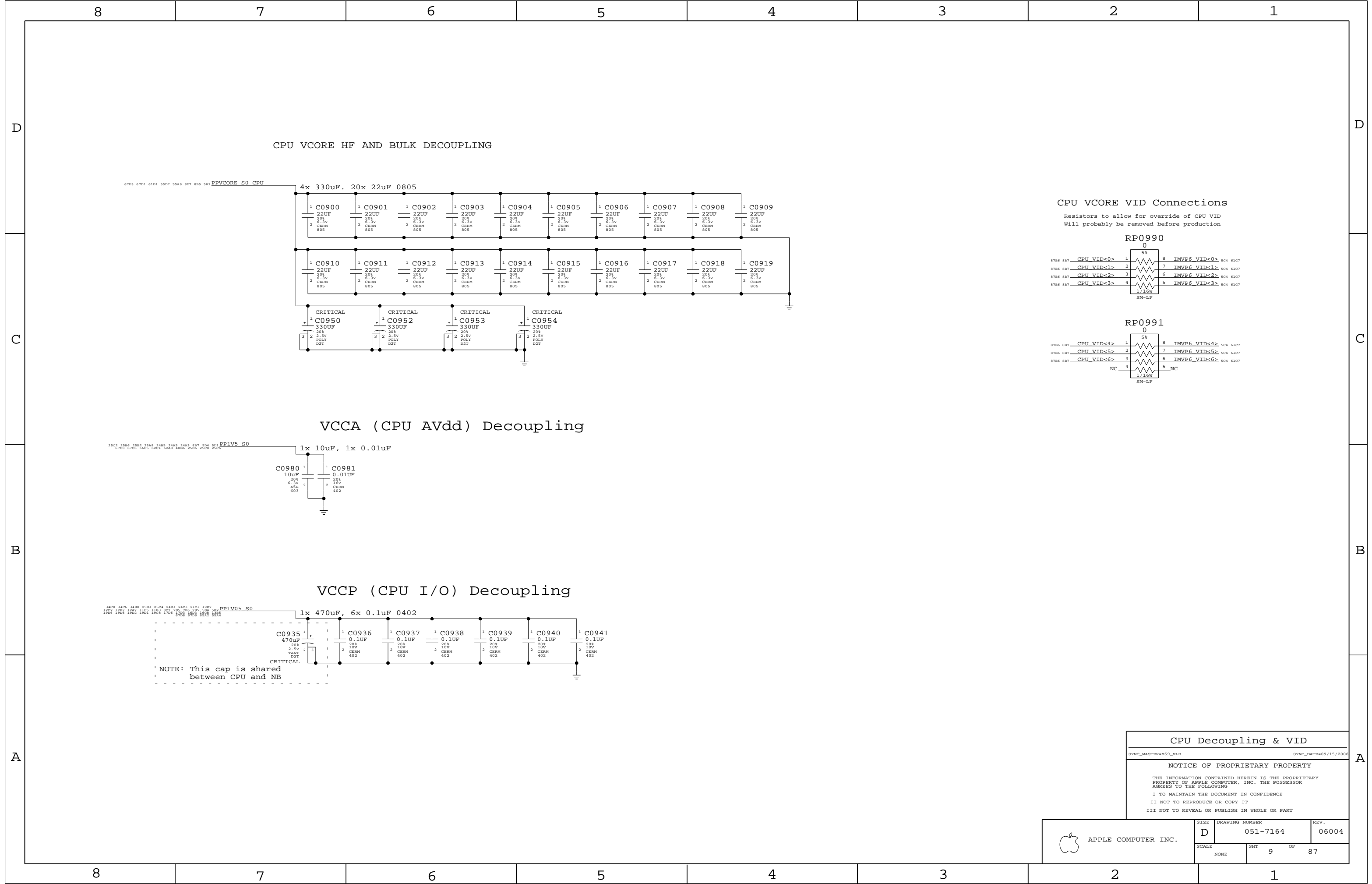












VCCA (CPU AVdd) Decoupling

25C2 25B6 25B2 25A8 24B6 24A1 24A3 8B7 5D4 5D1

PP1V5\_S0

1x 10uF, 1x 0.01uF

1 C0980 10uF 20% 6.3V X5R 603

2

1 C0981 0.01UF 20% 16V CERM 402

2

VCCP (CPU I/O) Decoupling

34C8 34C6 34B8 25D3 25C4 24D3 24C3 21C1 19D7

PP1V05\_S0

1x 470uF, 6x 0.1uF 0402

1 C0935 470uF 20% 2.5V TANT D2T

2

1 C0936 0.1UF 20% 10V CERM 402

2

1 C0937 0.1UF 20% 10V CERM 402

2

1 C0938 0.1UF 20% 10V CERM 402

2

1 C0939 0.1UF 20% 10V CERM 402

2

1 C0940 0.1UF 20% 10V CERM 402

2

1 C0941 0.1UF 20% 10V CERM 402

2

CRITICAL

NOTE: This cap is shared between CPU and NB

CPU VCORE VID Connections

Resistors to allow for override of CPU VID  
Will probably be removed before production

RP0990

0

5%

1 CPU VID<0>

2 CPU VID<1>

3 CPU VID<2>

4 CPU VID<3>

8 IMVP6 VID<0>

7 IMVP6 VID<1>

6 IMVP6 VID<2>

5 IMVP6 VID<3>

1/16W

SM-LF

RP0991

0

5%

1 CPU VID<4>

2 CPU VID<5>

3 CPU VID<6>

4 NC

8 IMVP6 VID<4>

7 IMVP6 VID<5>

6 IMVP6 VID<6>

5 NC

1/16W

SM-LF

CPU Decoupling & VID

SYNC\_MASTER=M59\_MLB

SYNC\_DATE=09/15/2006

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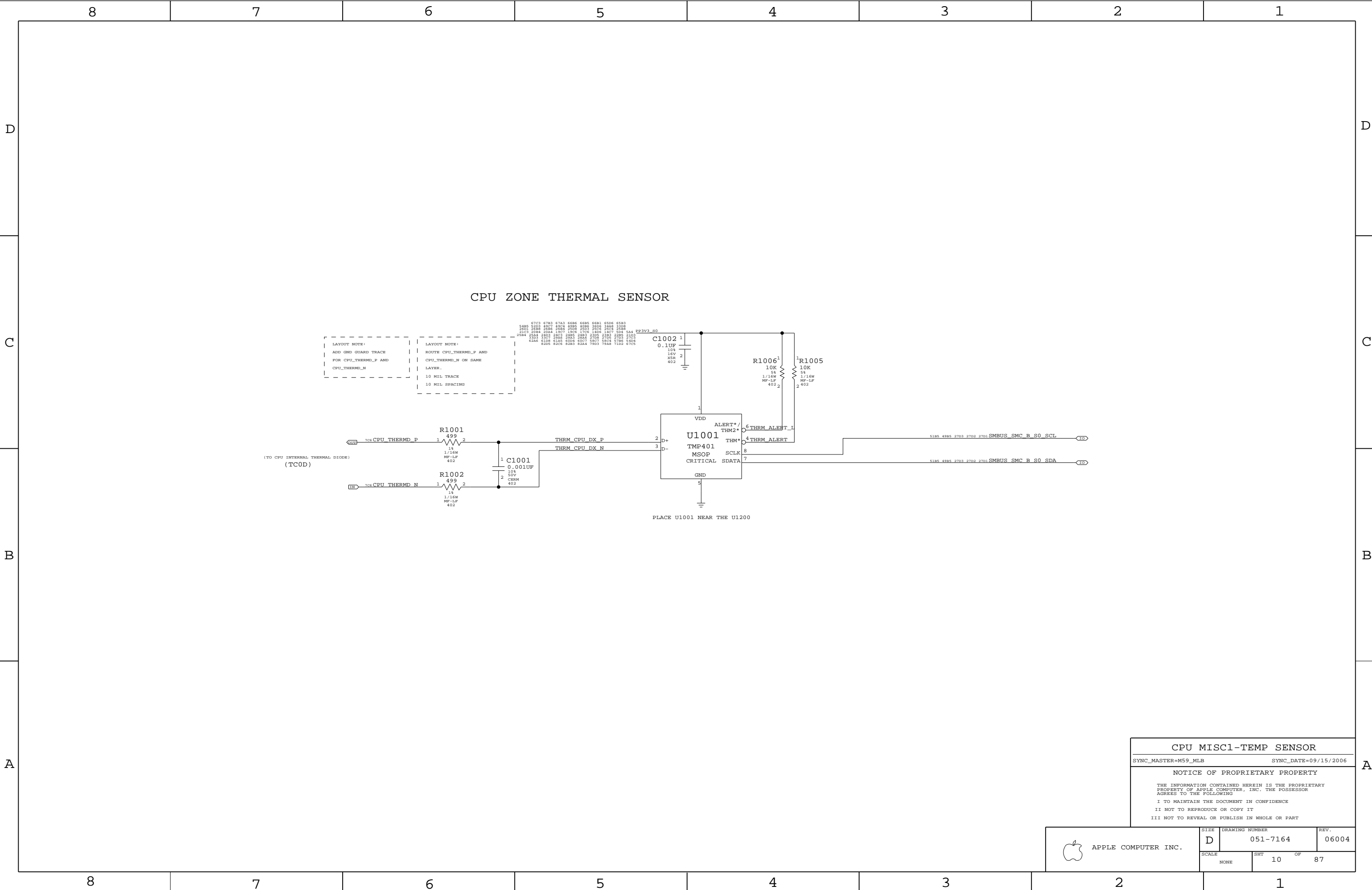
SIZE D

DRAWING NUMBER 051-7164

REV. 06004

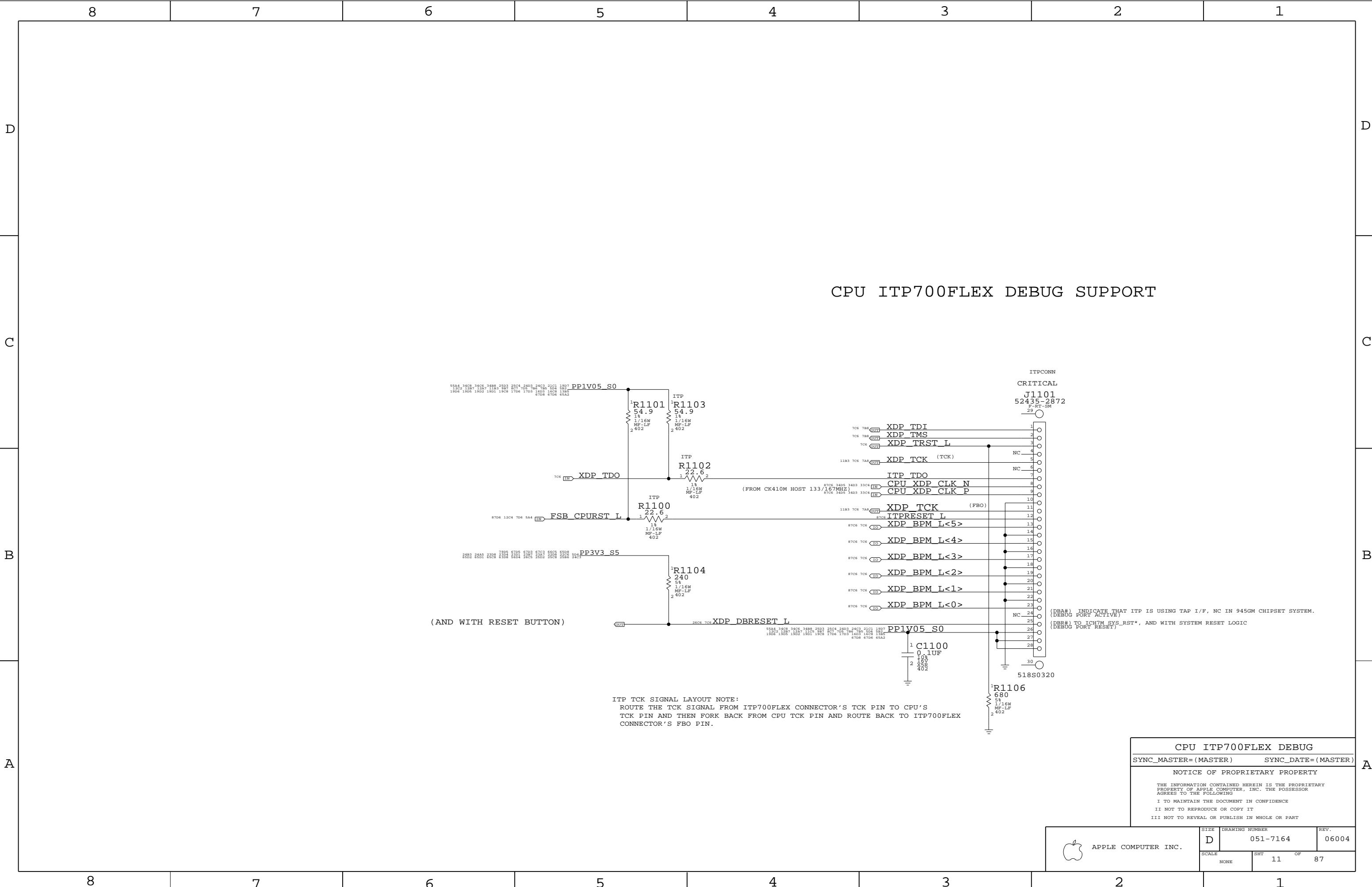
SCALE NONE

SHT 9 OF 87



CPU MISC1-TEMP SENSOR		
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CPU ITP700FLEX DEBUG

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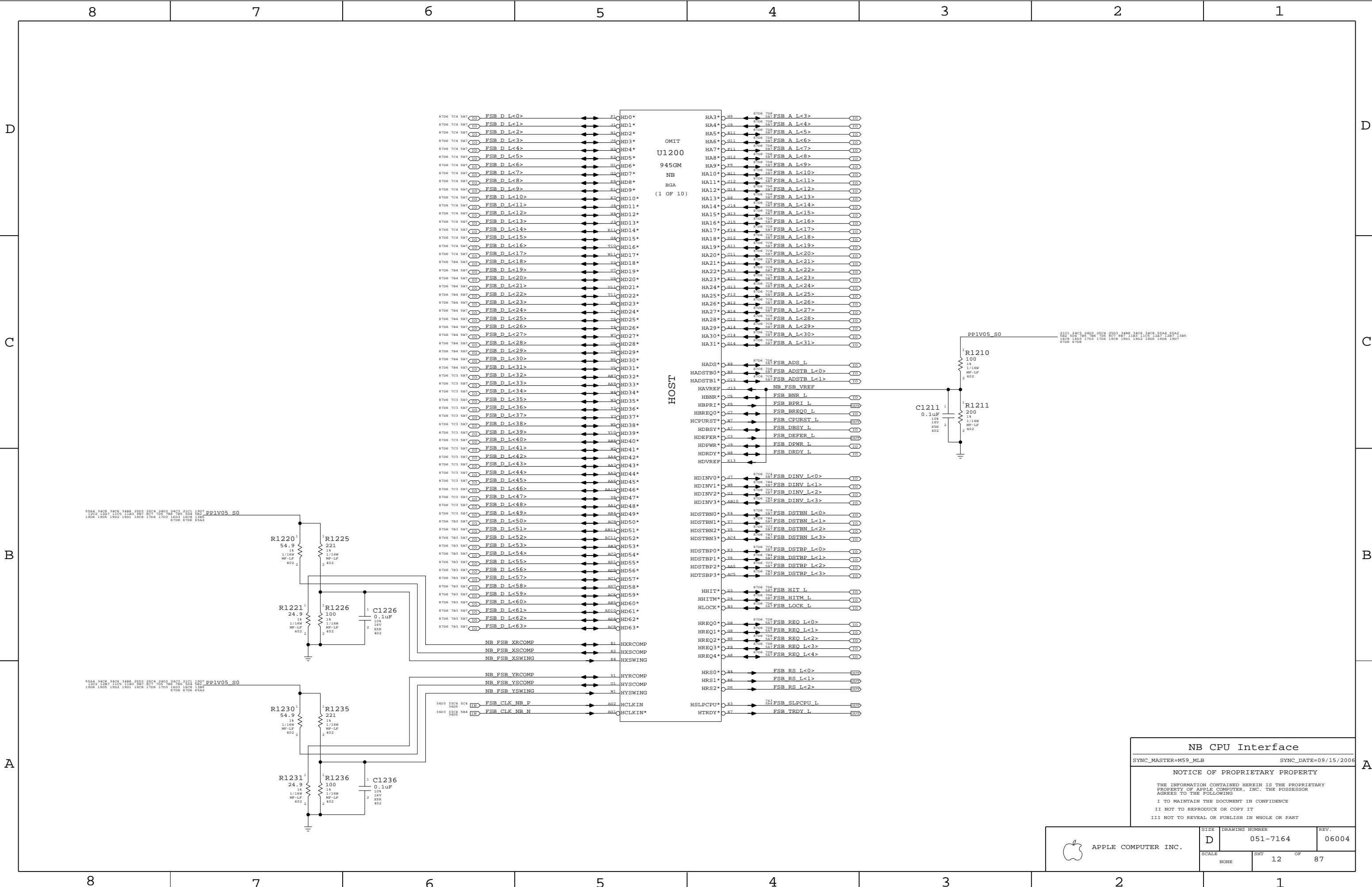
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NONE		11	87



NB CPU Interface

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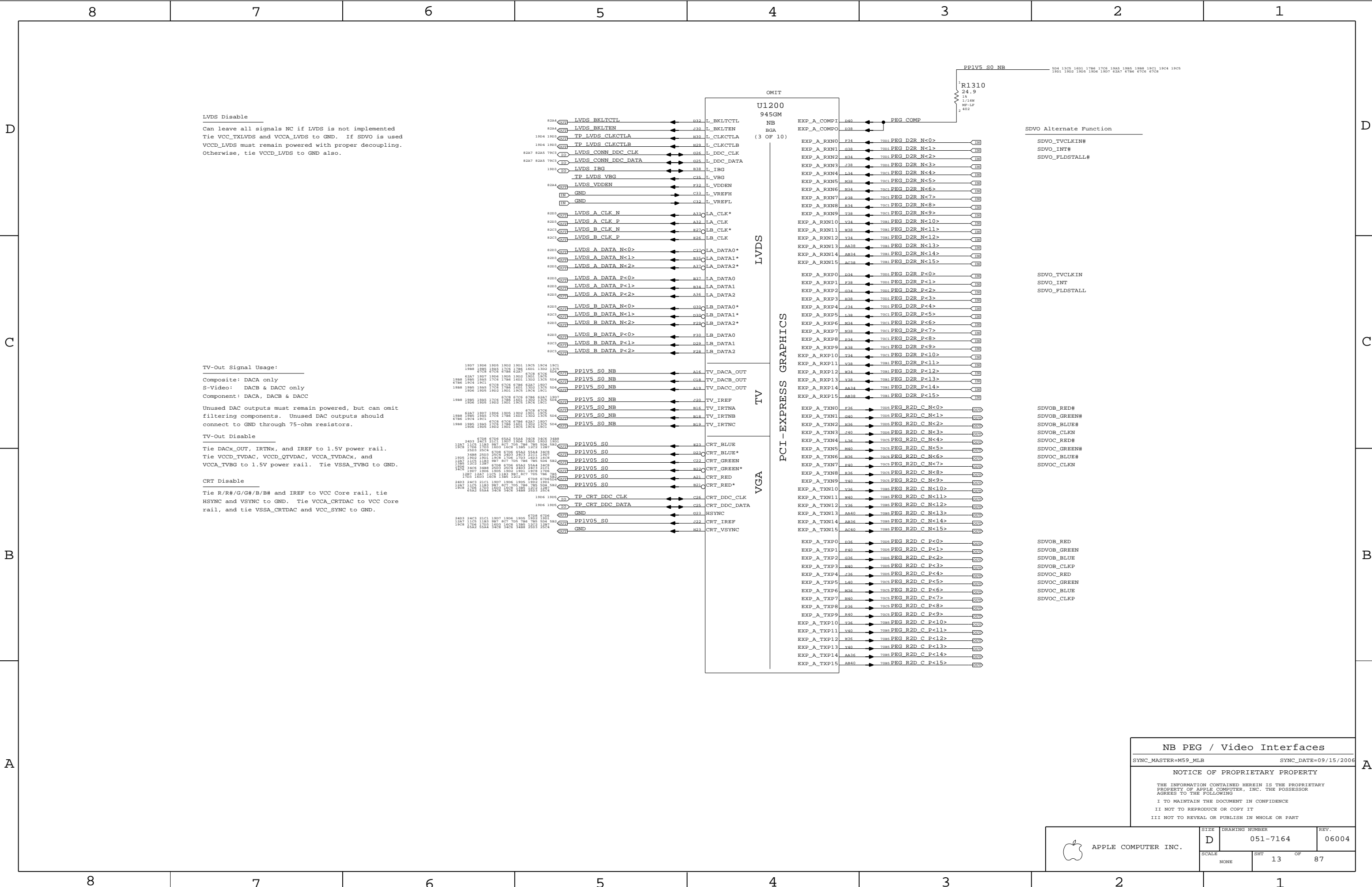
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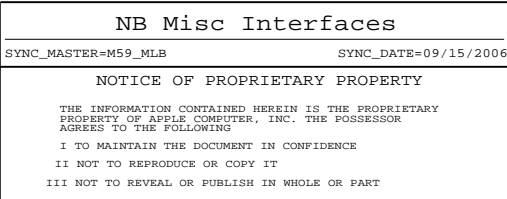
NB PEG / Video Interfaces

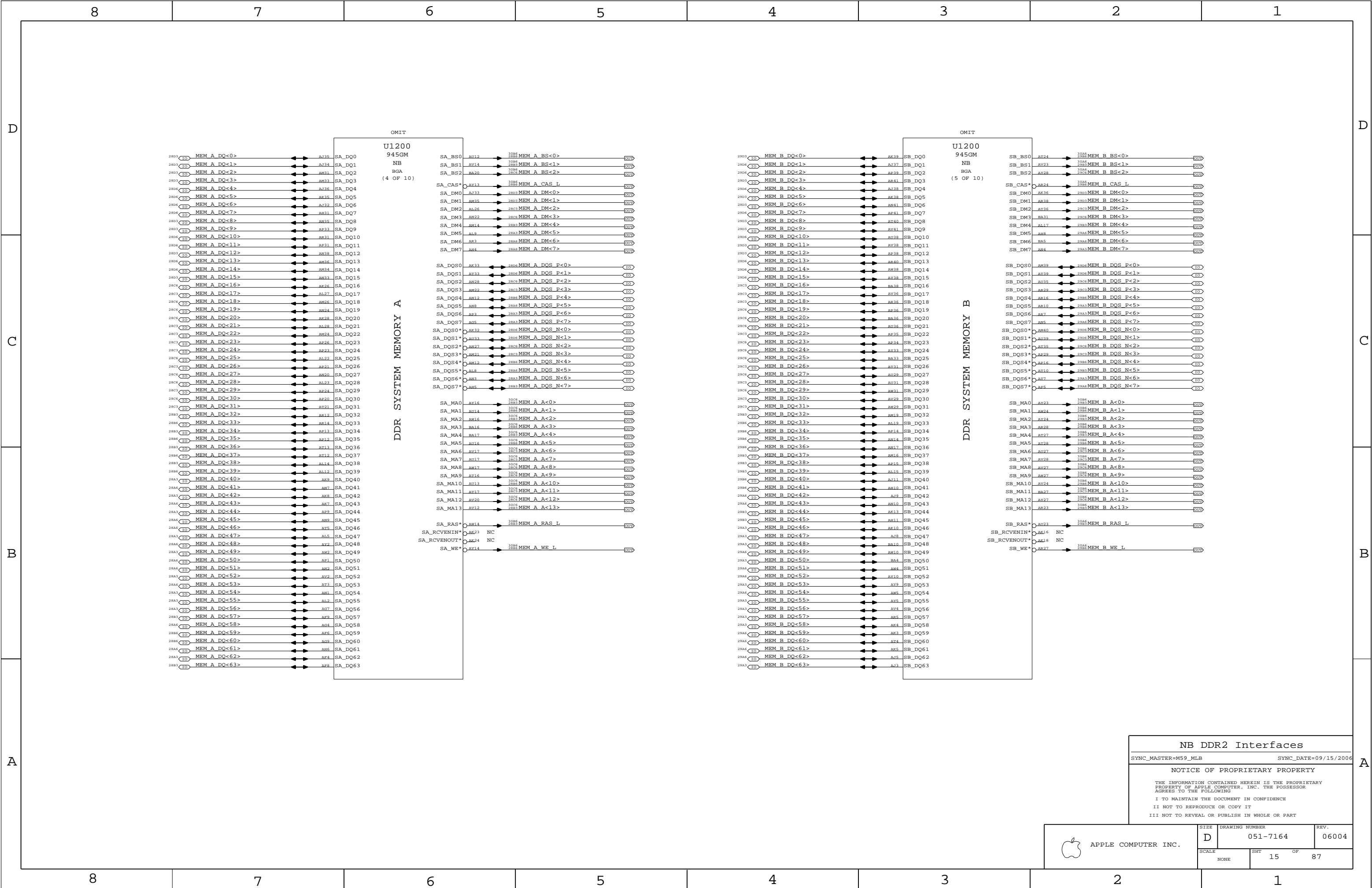
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NB DDR2 Interfaces

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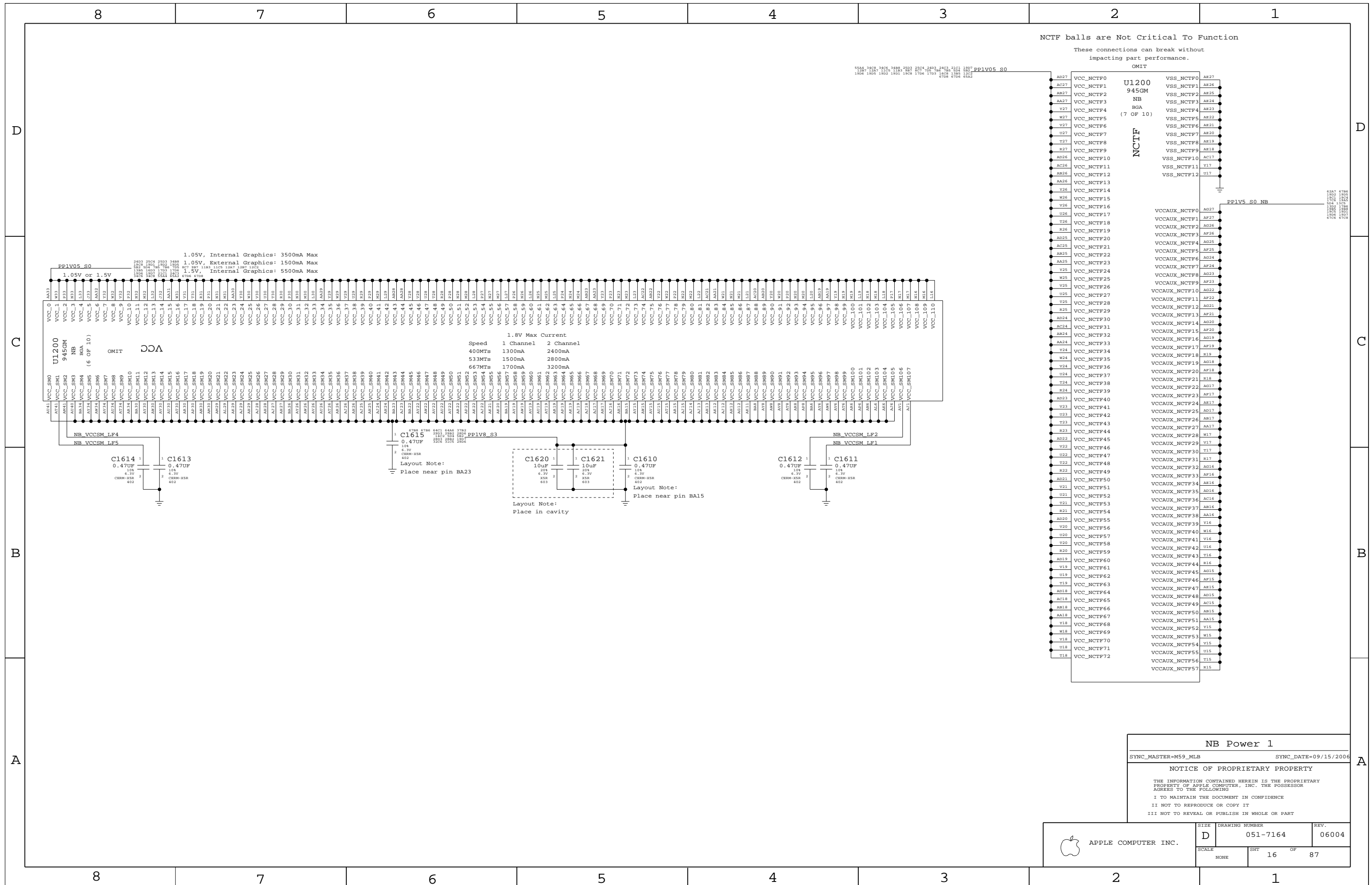
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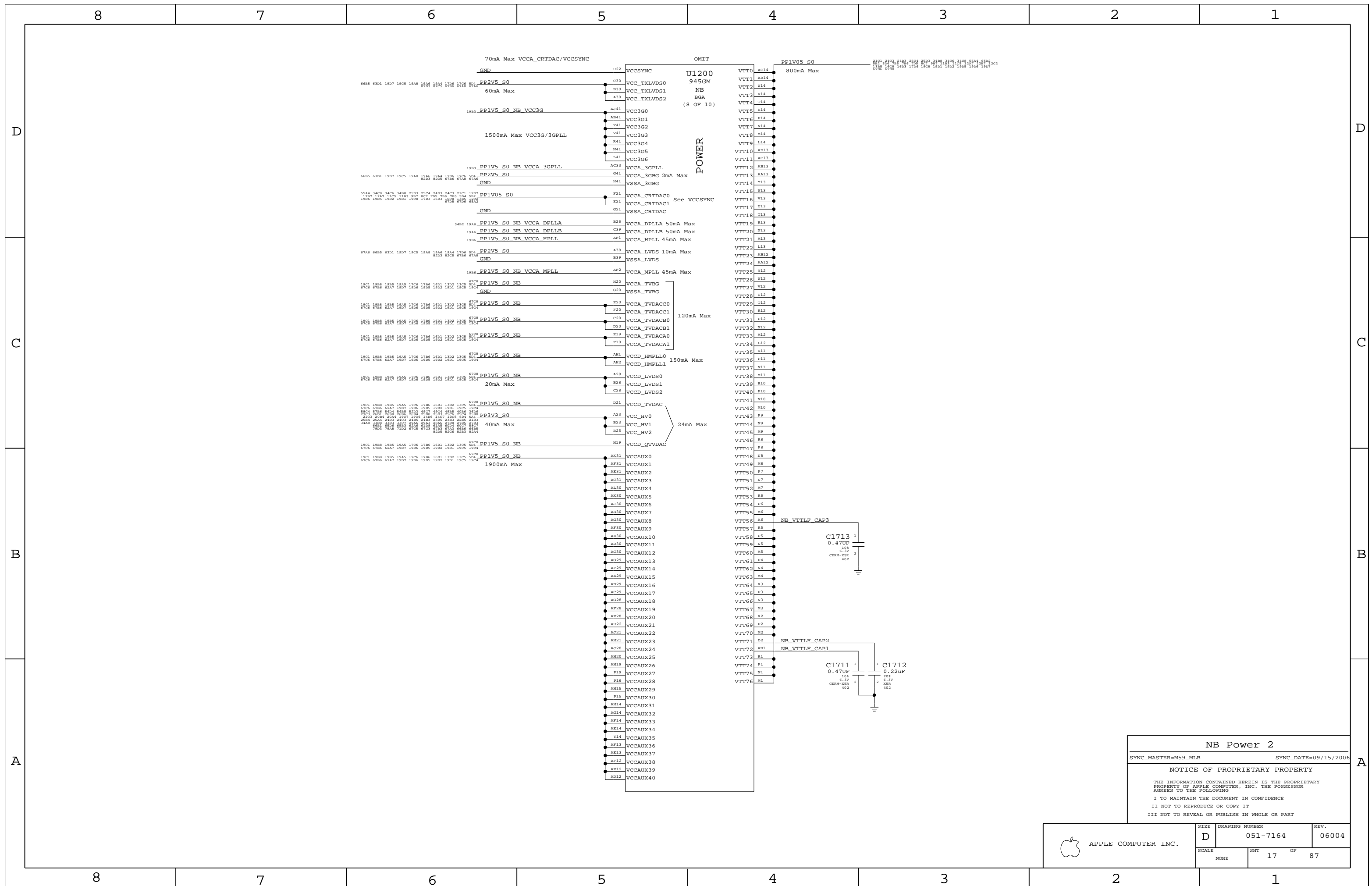
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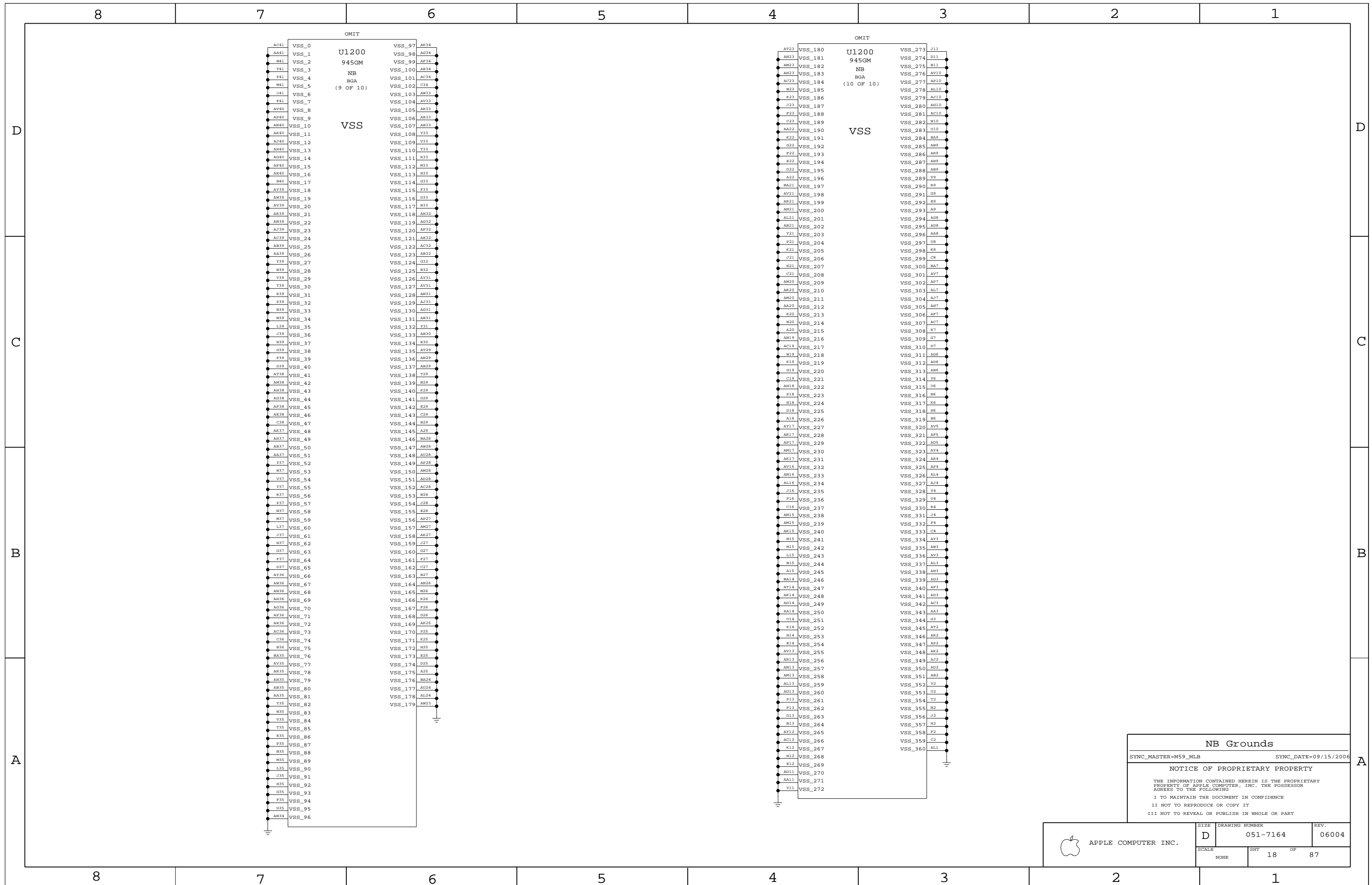
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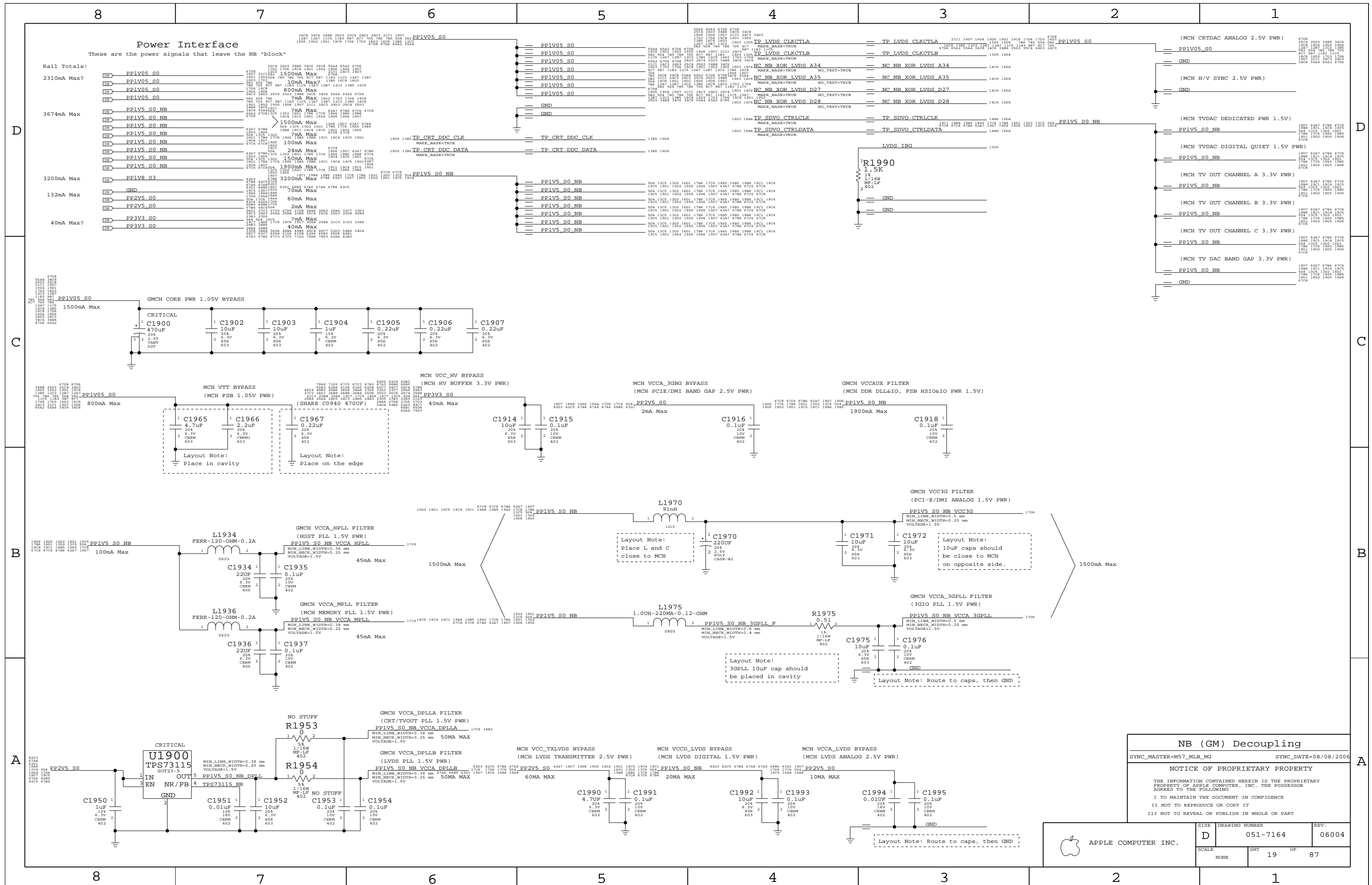
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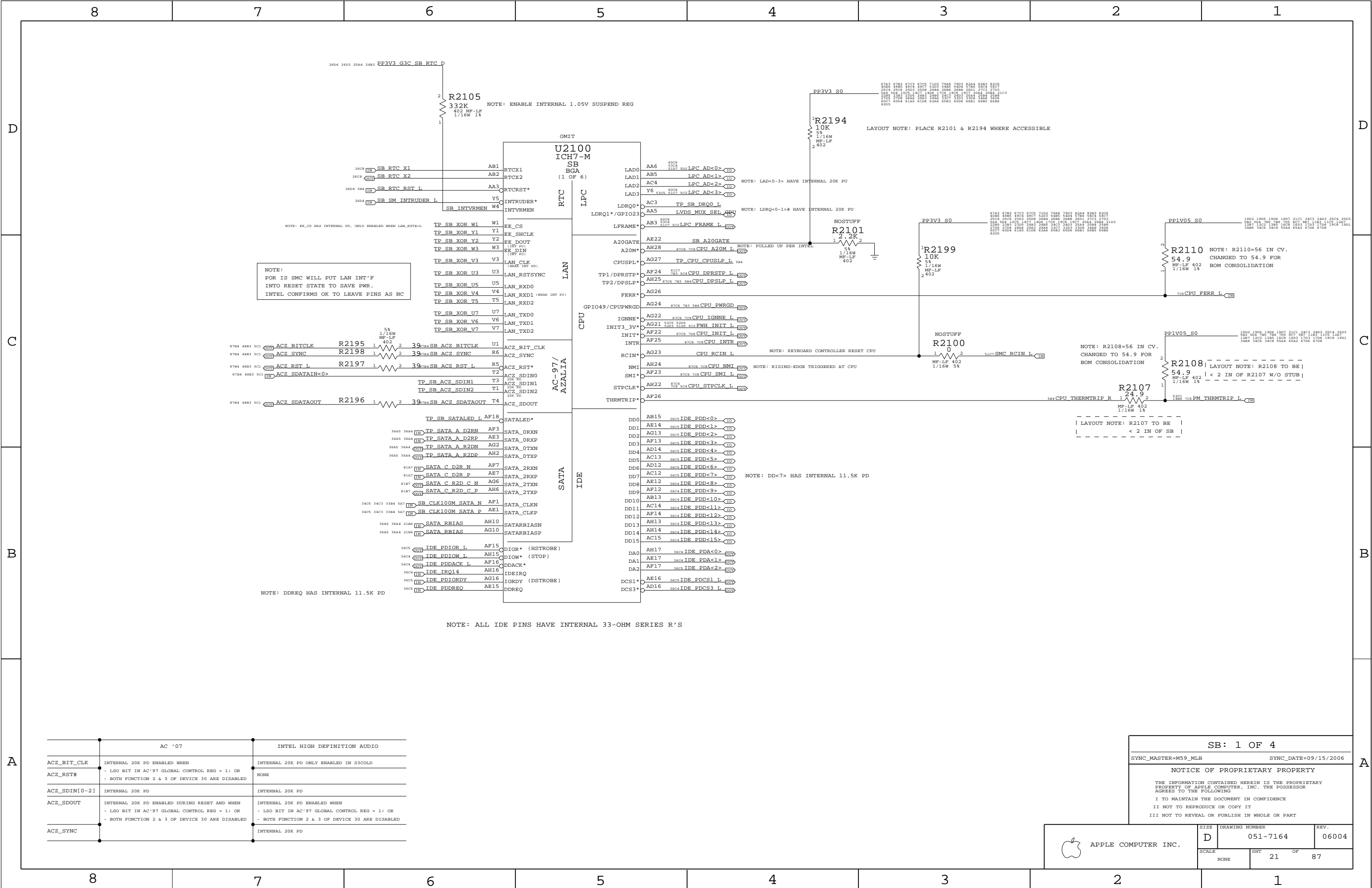








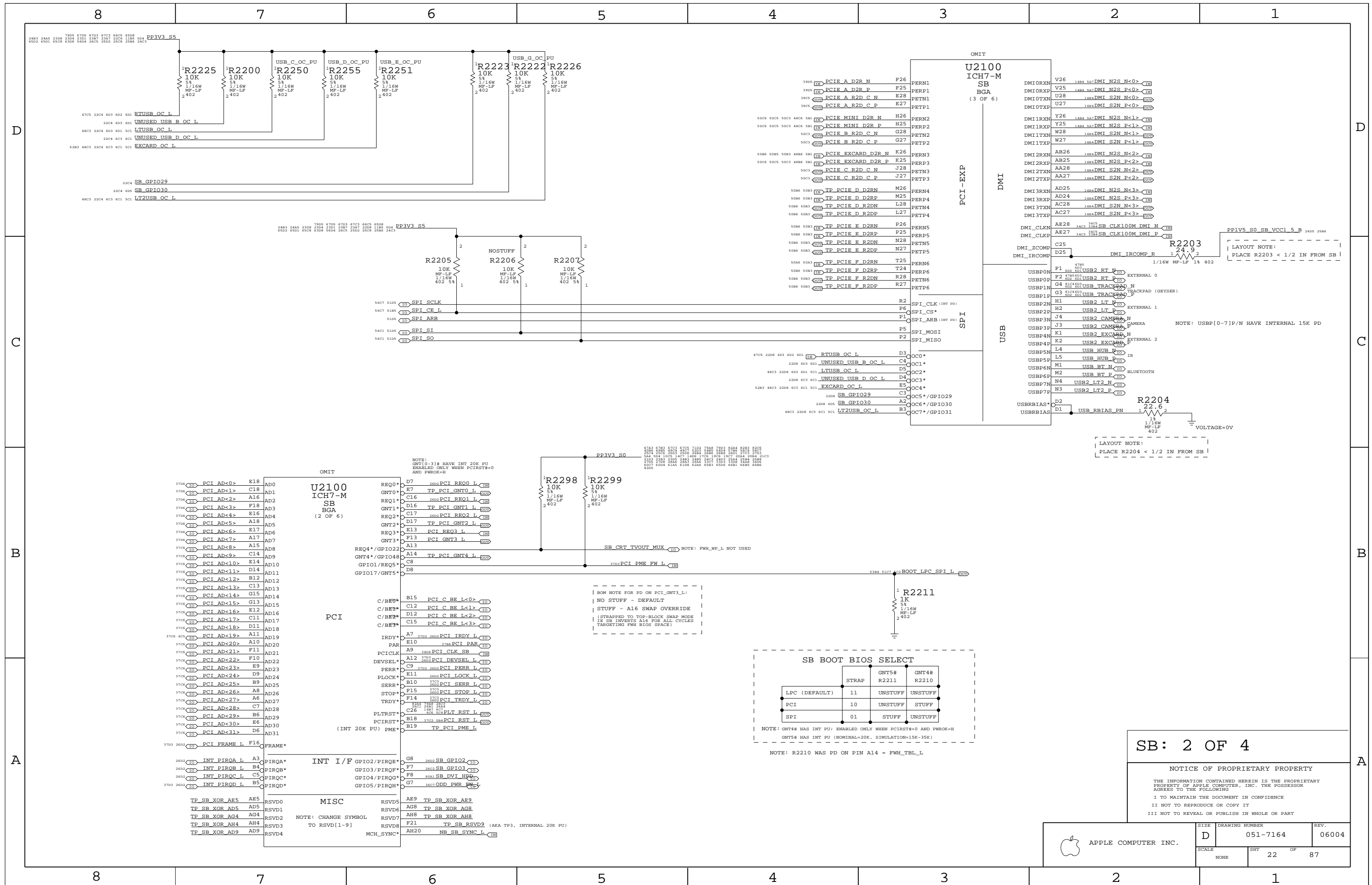


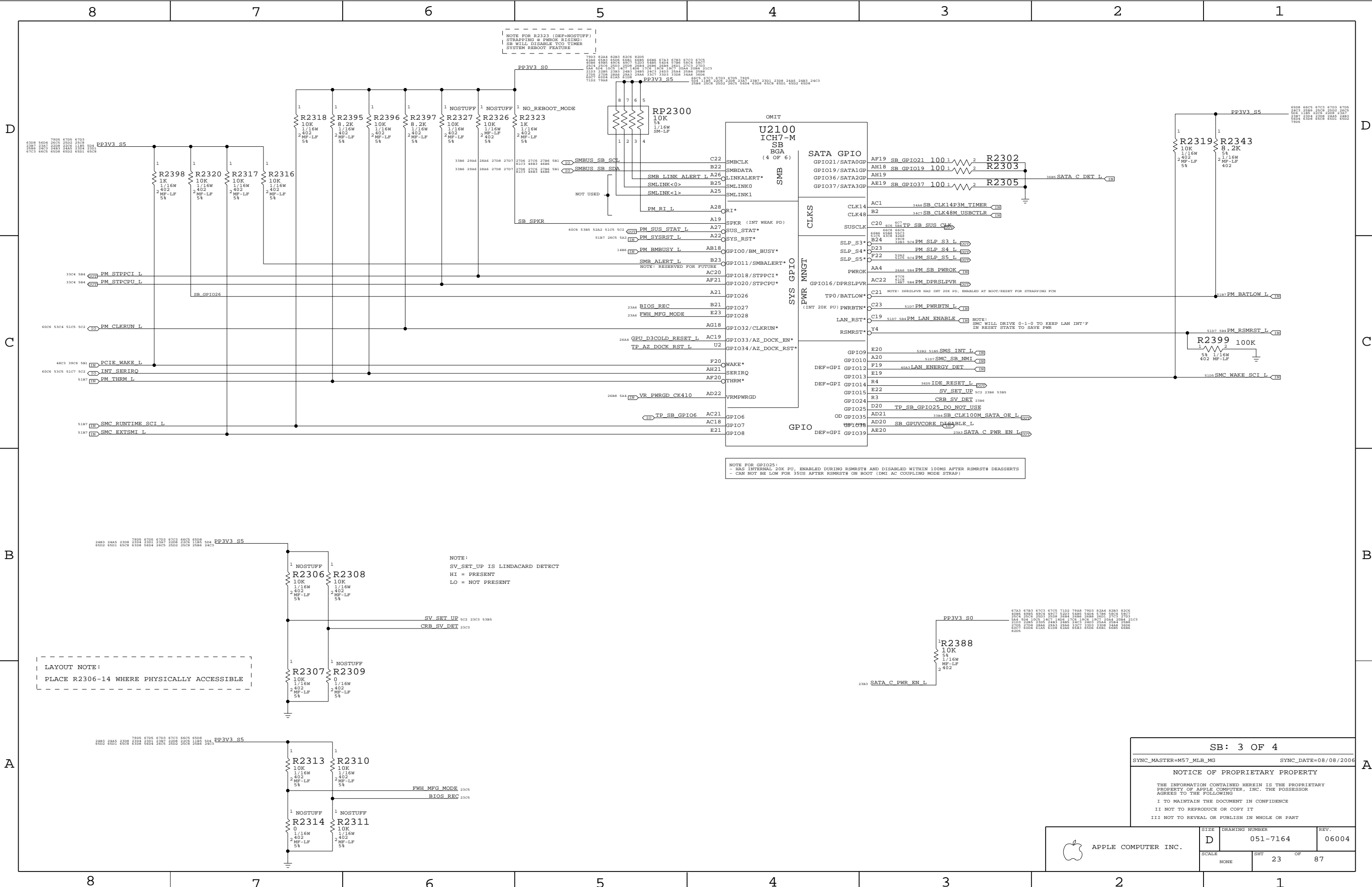


	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4		
SYNC_MASTER=M59_MLB		SYNC_DATE=09/15/2006
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SCALE		SHT	OF
NONE		21	87





NOTE FOR R2323 (DEF-NOSTUFF):  
STRAPPING & PWROK RISING:  
SB WILL DISABLE TCO TIMER  
SYSTEM REBOOT FEATURE

NOTE FOR GPIO25:  
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS  
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

LAYOUT NOTE:  
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

NOTE:  
SV\_SET\_UP IS LINDACARD DETECT  
HI = PRESENT  
LO = NOT PRESENT

SB: 3 OF 4

SYNC\_MASTER=M57\_MLB\_MG SYNC\_DATE=08/08/2006

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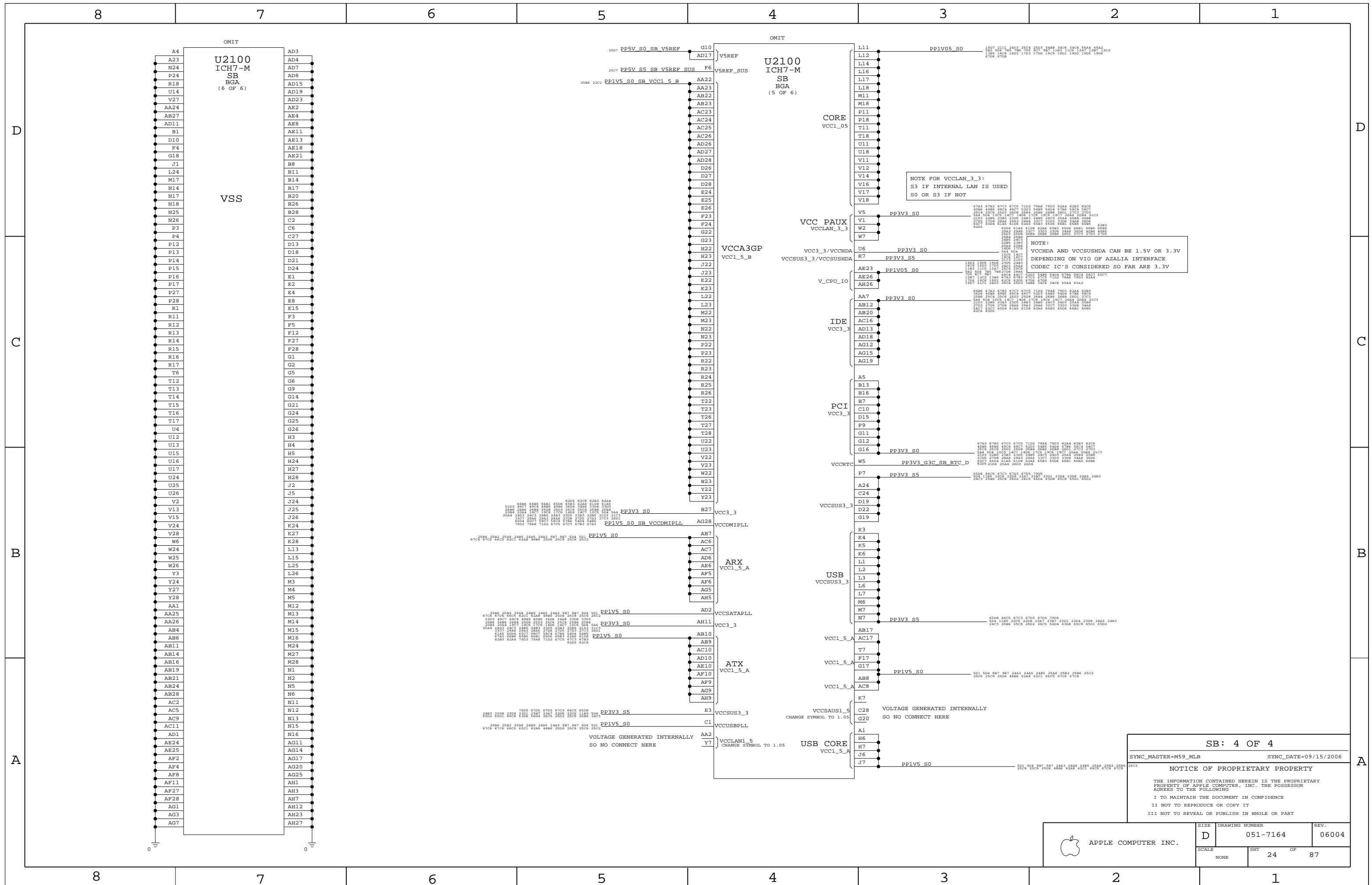
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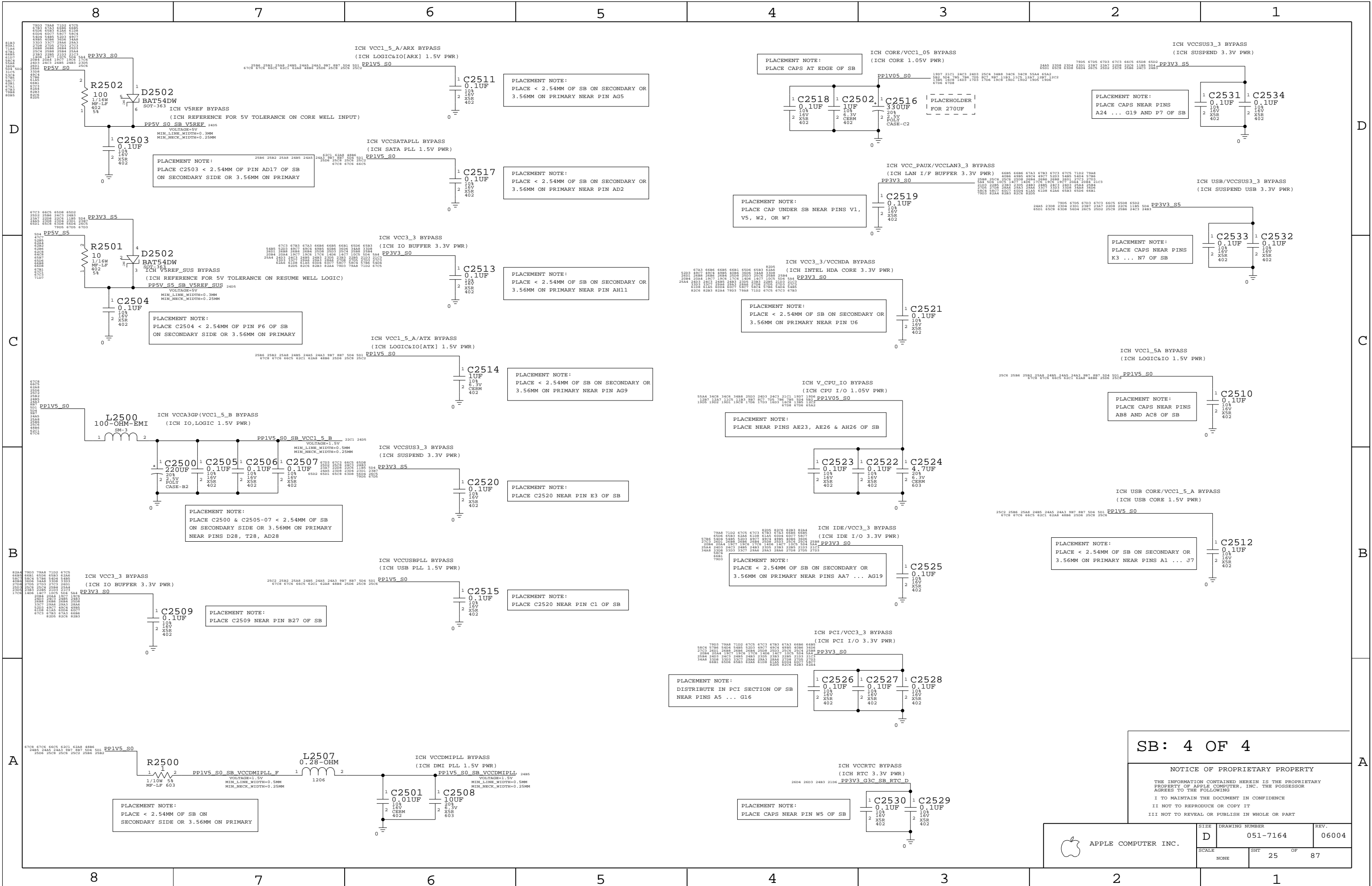
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NONE		23	87







SB: 4 OF 4

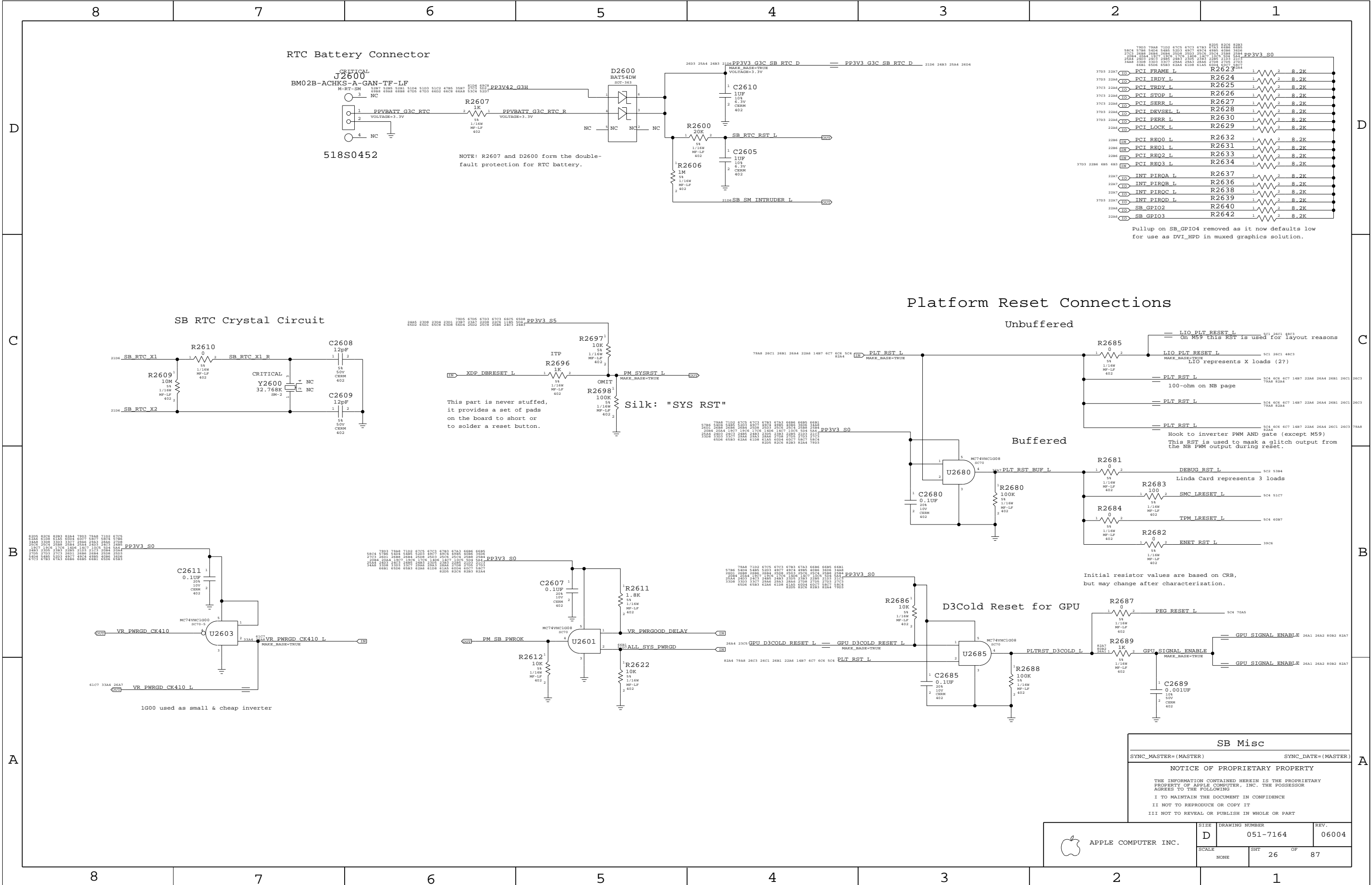
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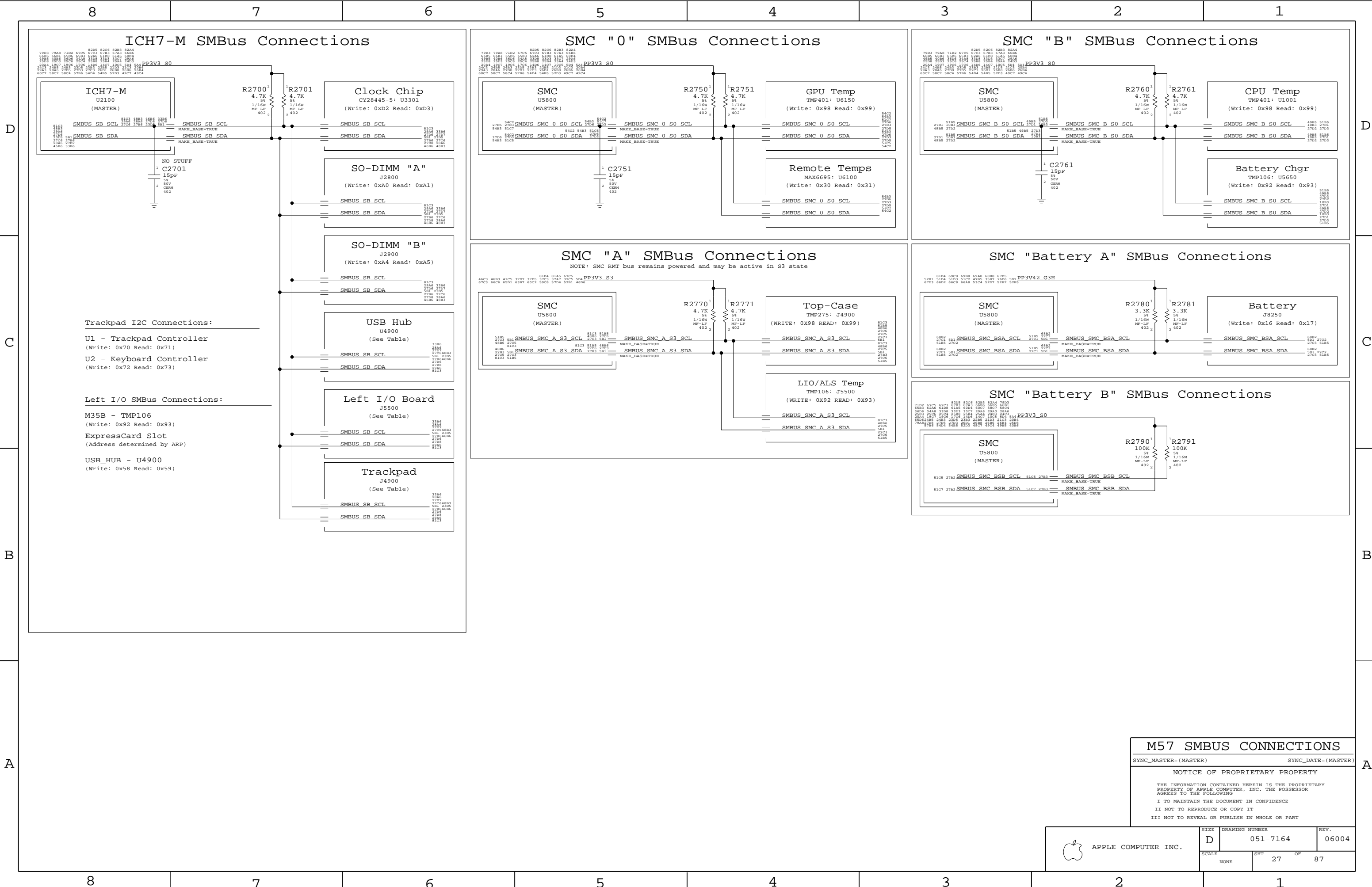
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NONE	25	87





M57 SMBUS CONNECTIONS

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SIZE

D

DRAWING NUMBER

051-7164

REV.

06004

SCALE

NONE

SHT

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Power aliases required by this page:

- =PP1V8\_S3\_MEM
- =PPSPD\_S0\_MEM (2.5V ~ 3.3V)

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Signal aliases required by this page:

- =I2C\_SODIMMA\_SCL
- =I2C\_SODIMMA\_SDA

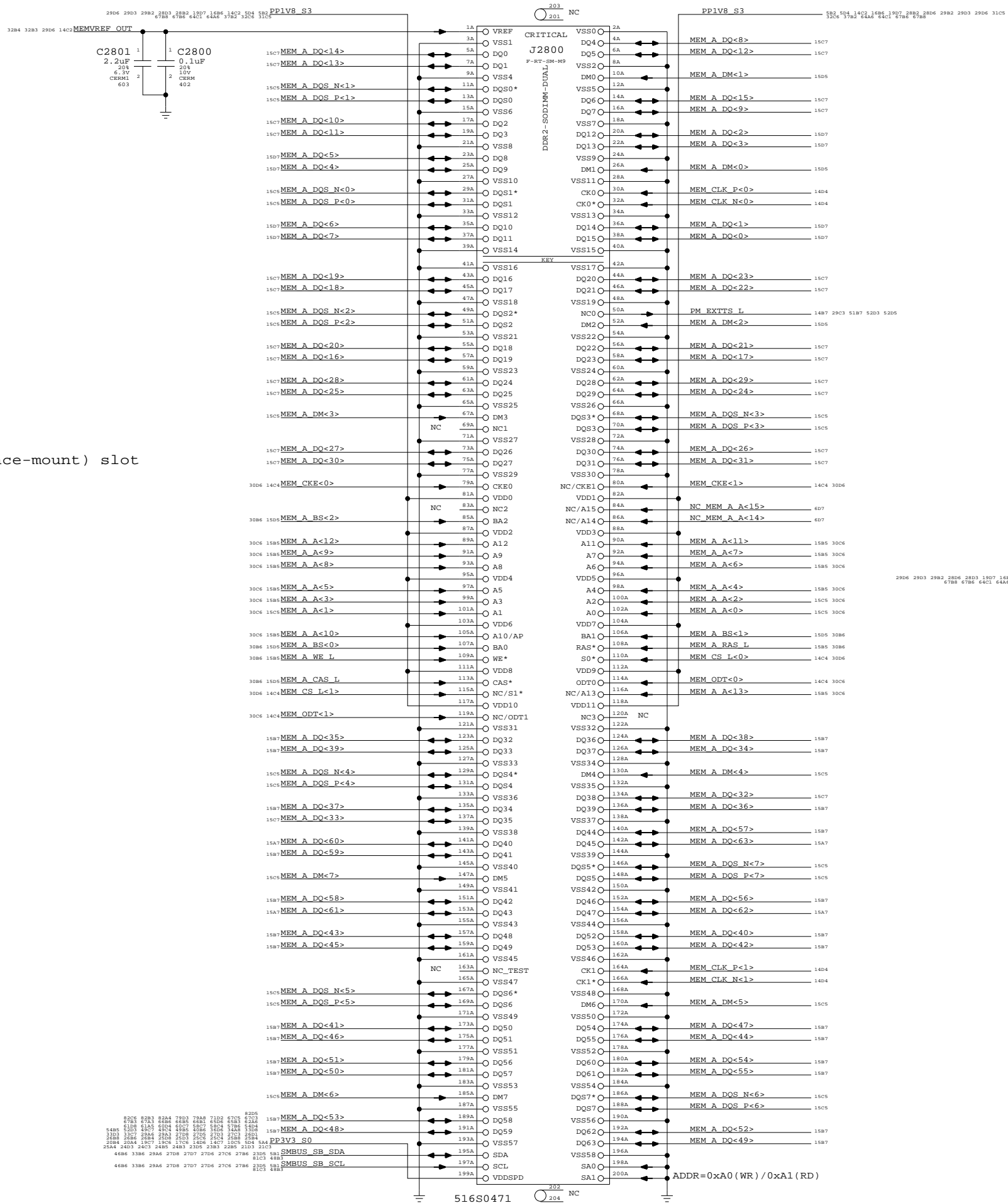
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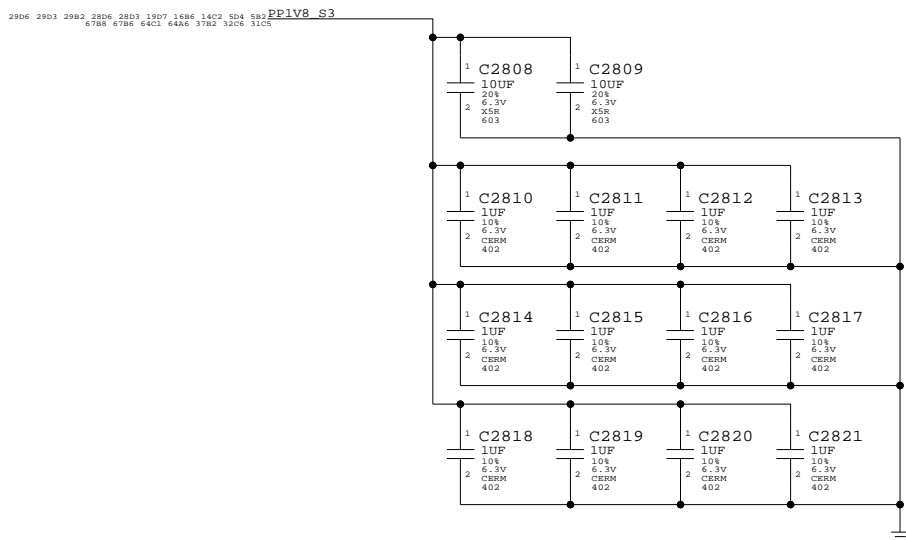
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by another page.

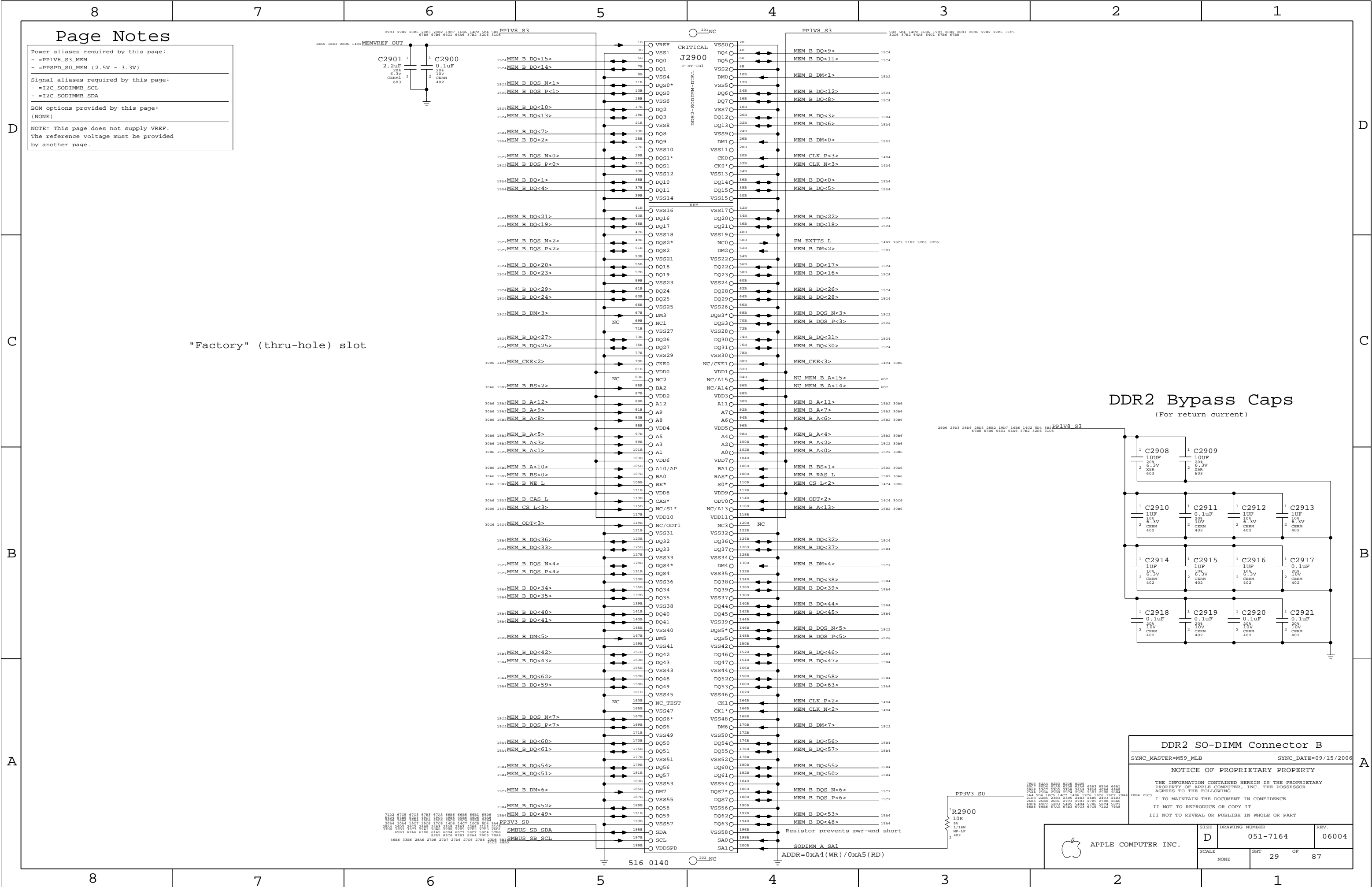


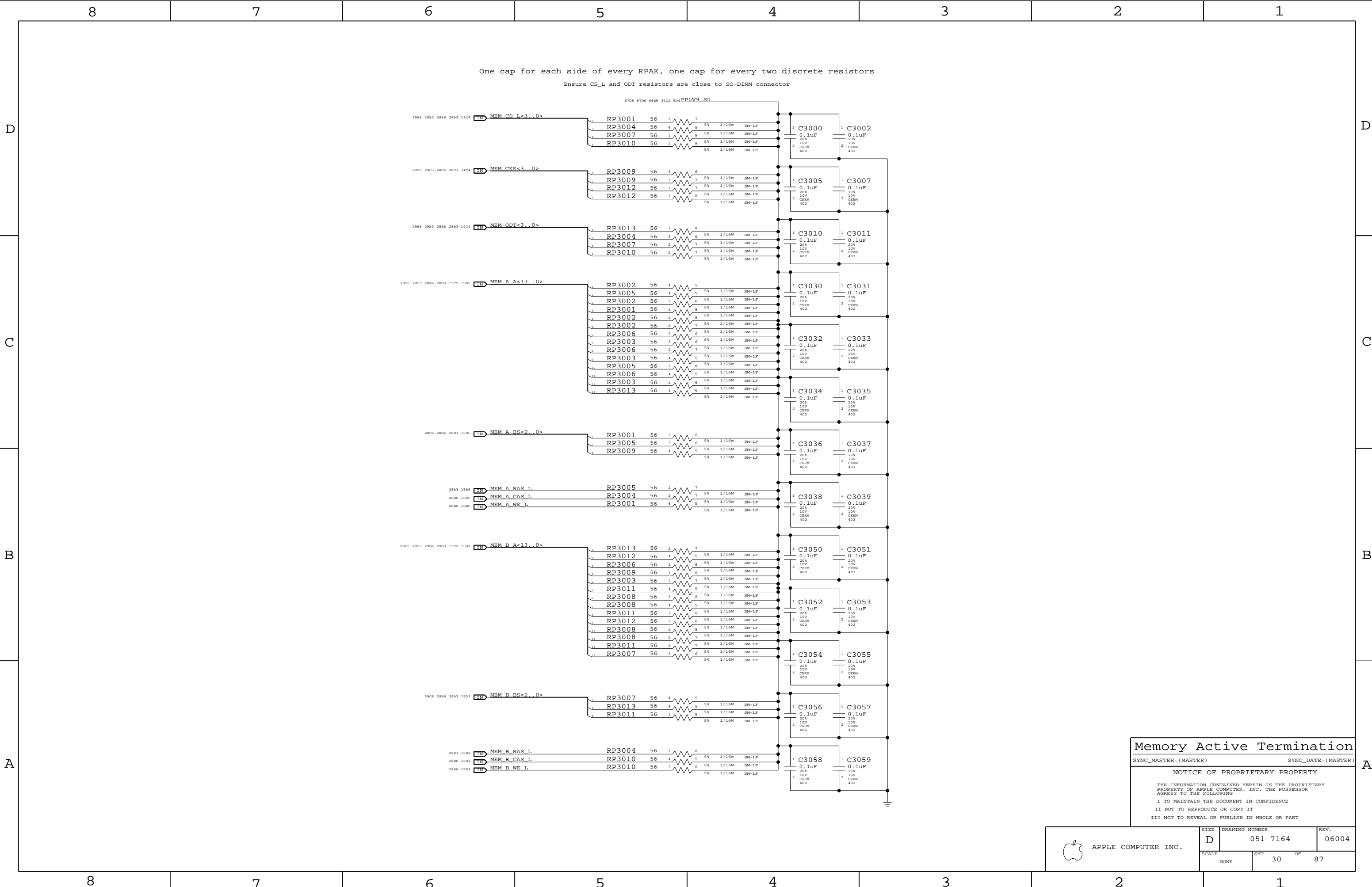
(For return current)



DDR2 SO-DIMM Connector A	
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Memory Active Termination

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SCALE

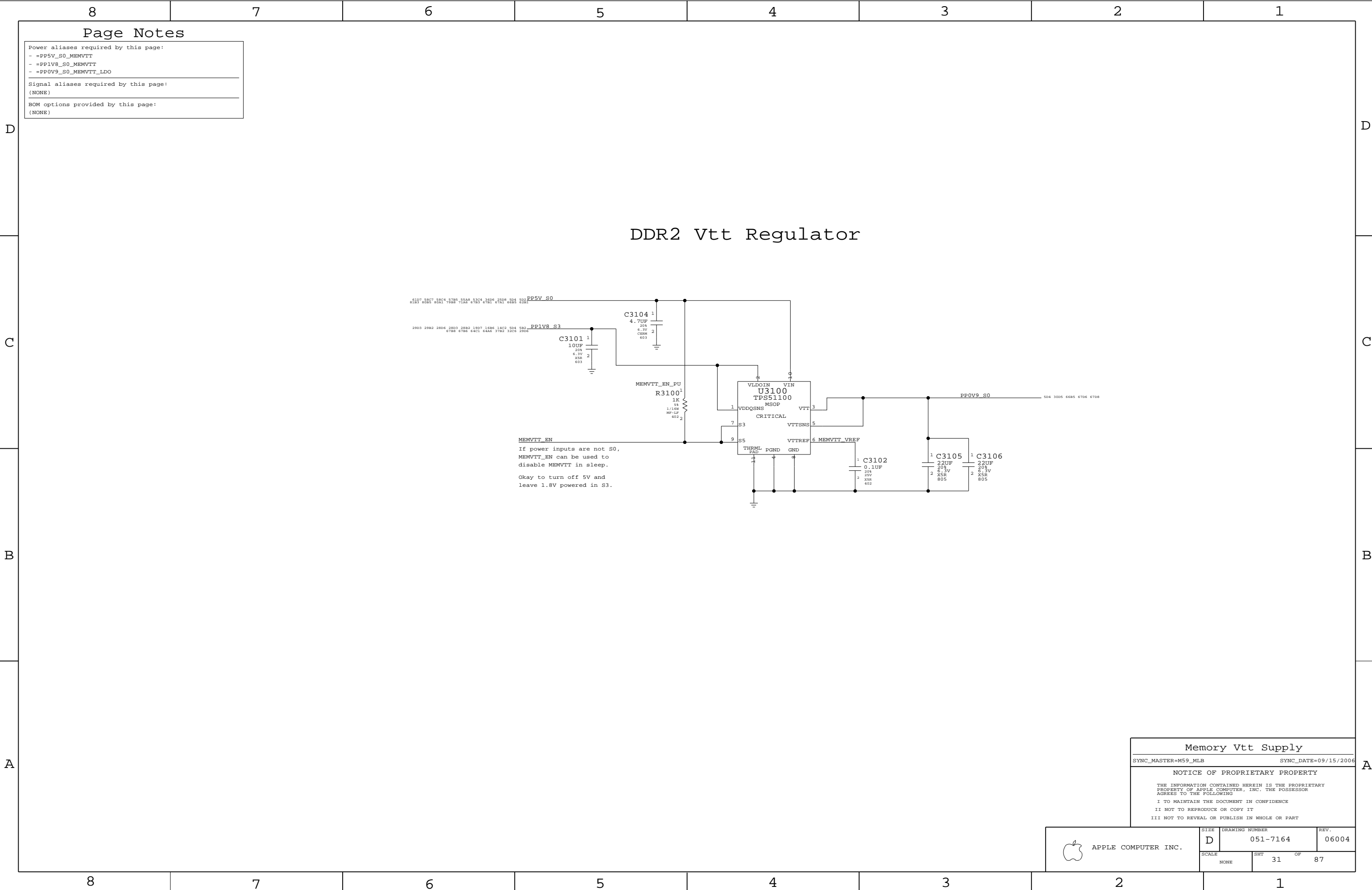
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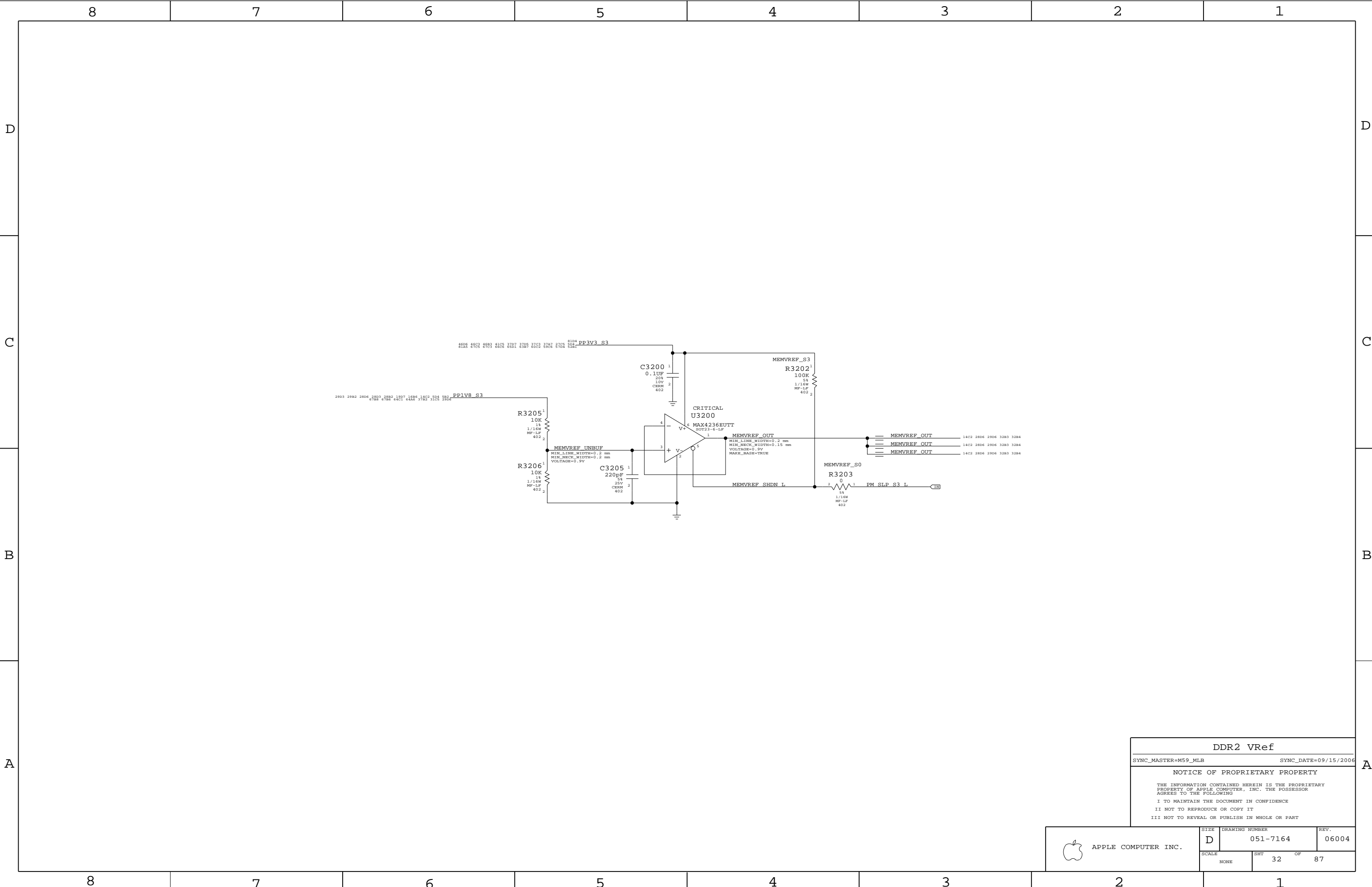
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DDR2 VRef

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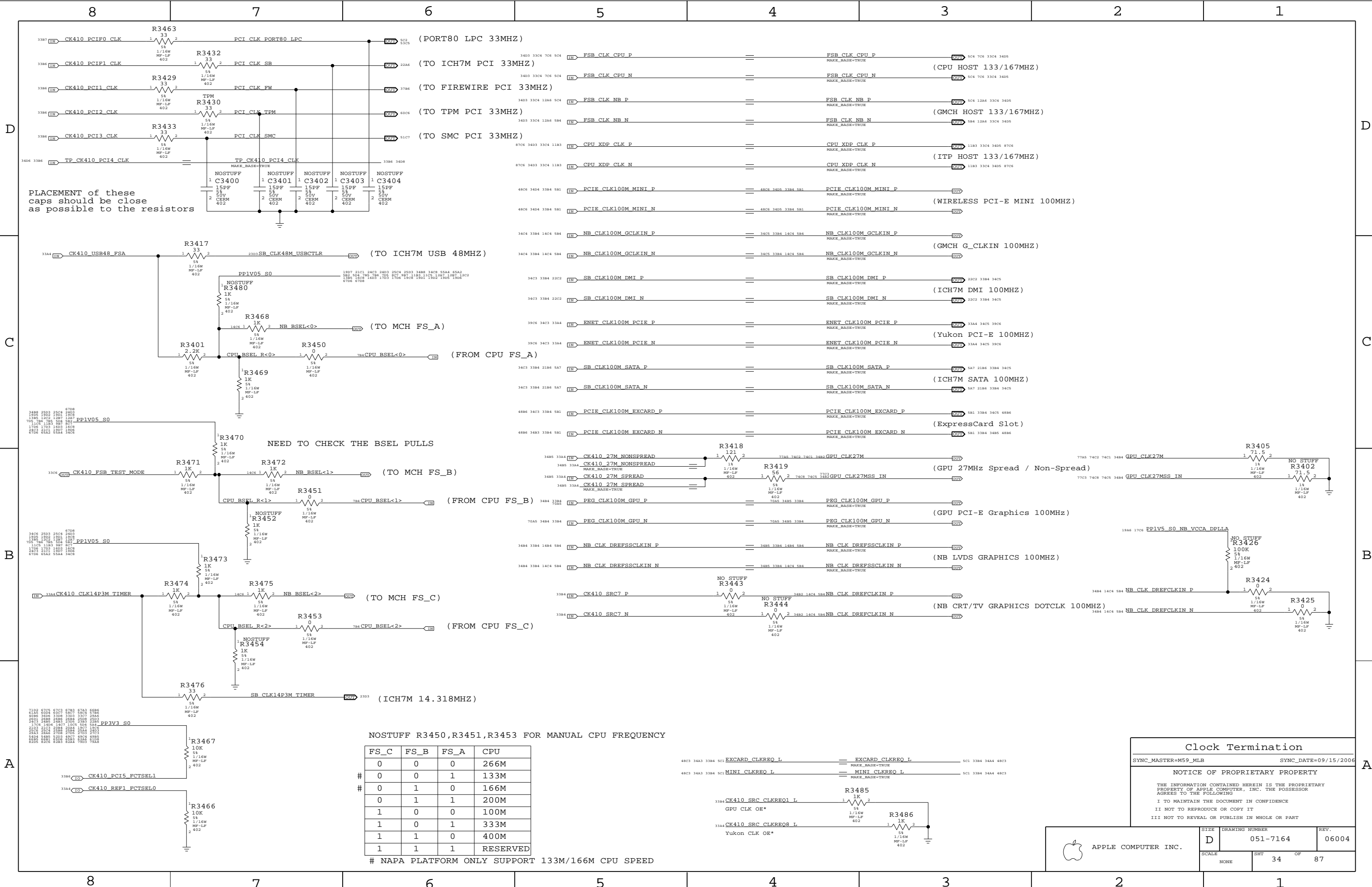
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SCALE		SHT	OF
NONE		32	87







PLACEMENT of these caps should be close as possible to the resistors

NEED TO CHECK THE BSEL PULLS

NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
#	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
#	0	1	1	200M
#	1	0	0	100M
#	1	0	1	333M
#	1	1	0	400M
#	1	1	1	RESERVED

# NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED

Clock Termination

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SYNC\_DATE=09/15/2006

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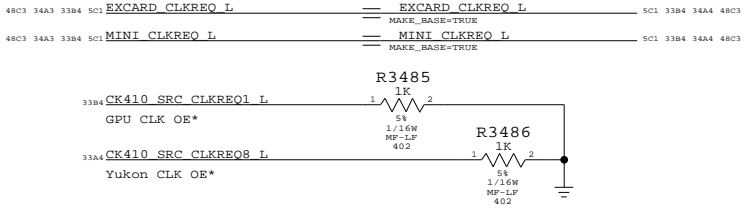
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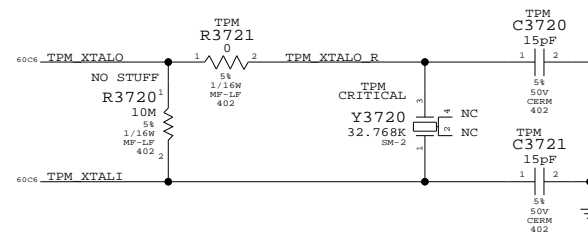
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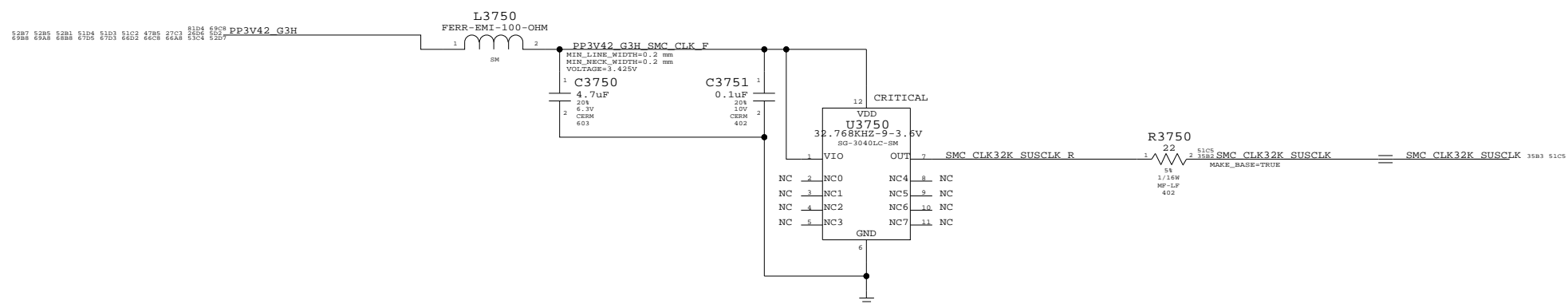
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## TPM Crystal Circuit



## SMC G3Hot Oscillator



Mobile Clocking

SYNC_MASTER=M59_MLB	SYNC_DATE=09/15/2006
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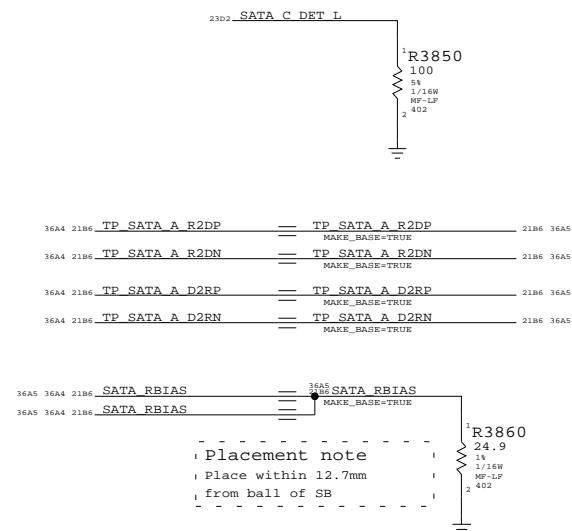
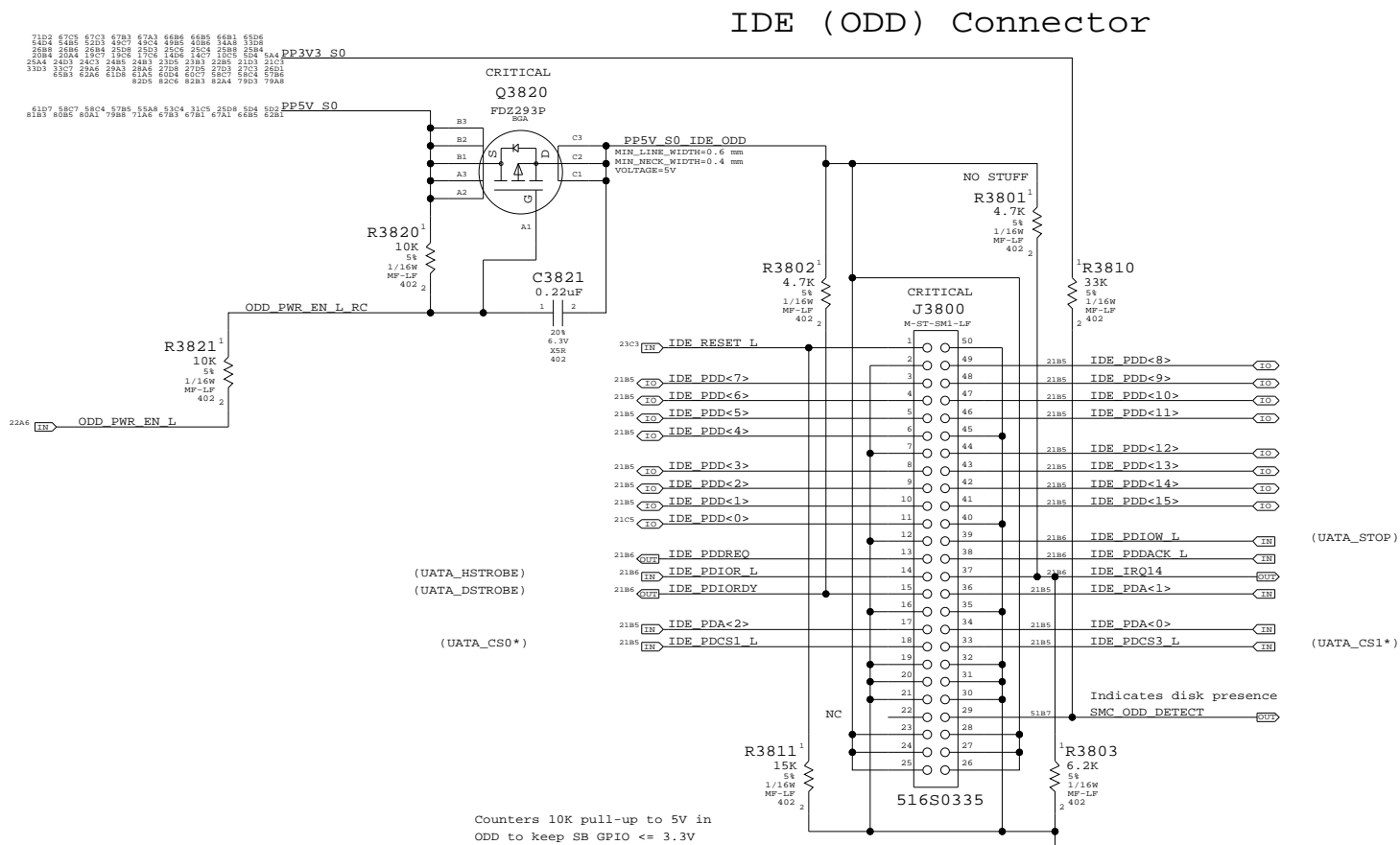
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06004
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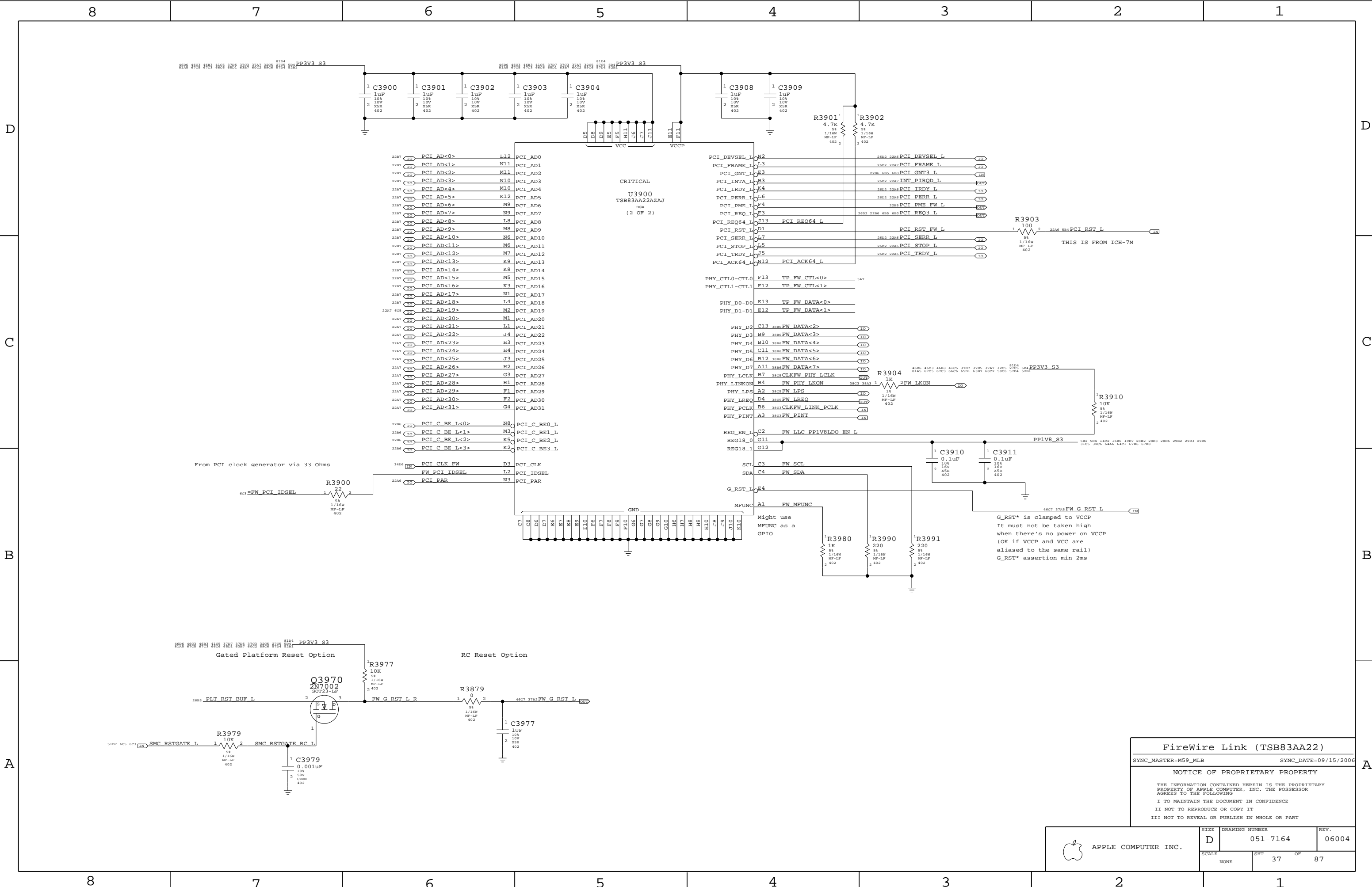
SHT	3
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<h1>PATA Connector</h1>	
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	NONE	36	87



FireWire Link (TSB83AA22)

SYNC\_MASTER=M59\_MLB

SYNC\_DATE=09/15/2006

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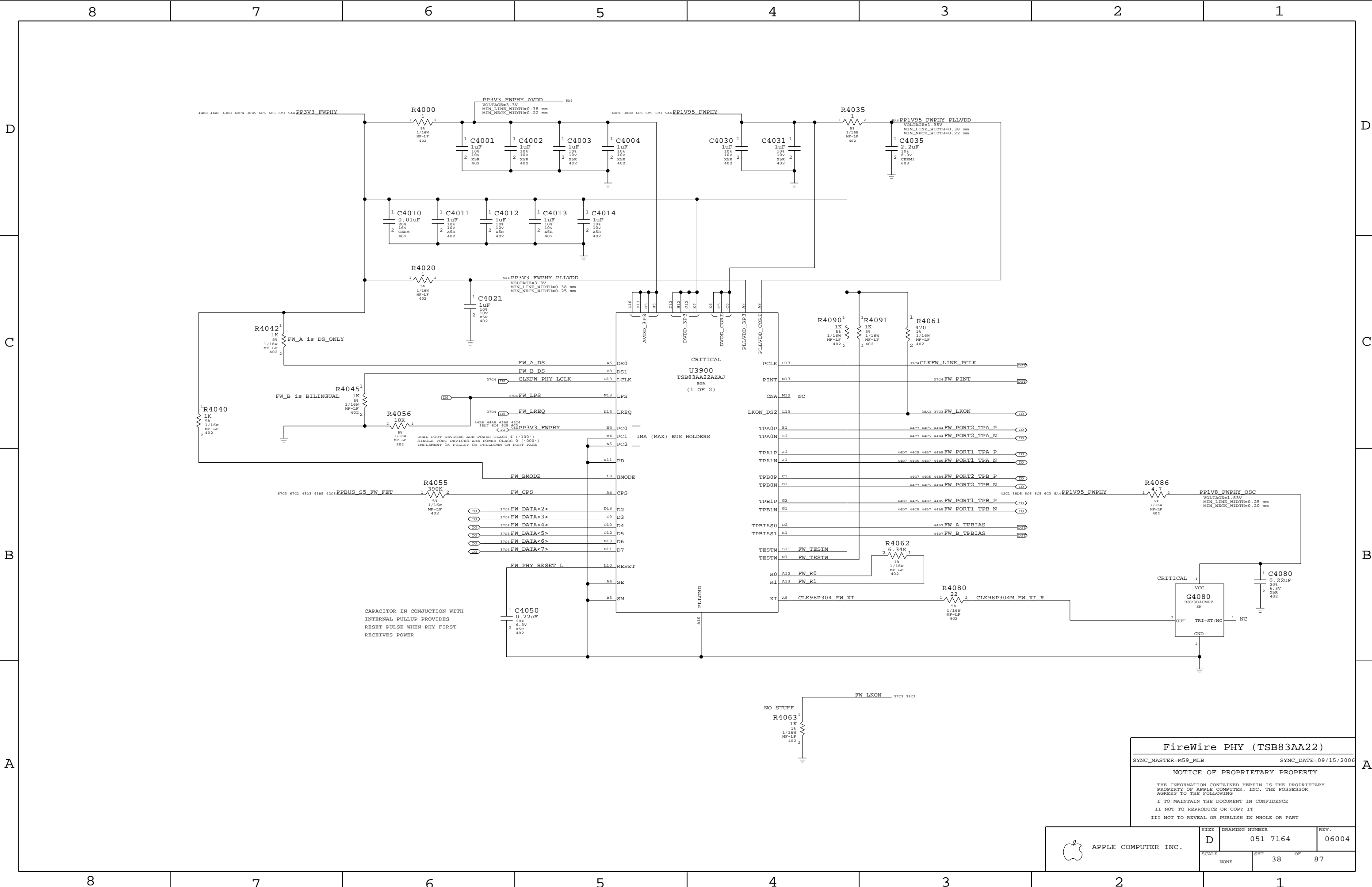
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NONE		37	87



FireWire PHY (TSB83AA22)

SYNC\_MASTER=M59\_MLB

SYNC\_DATE=09/15/2006


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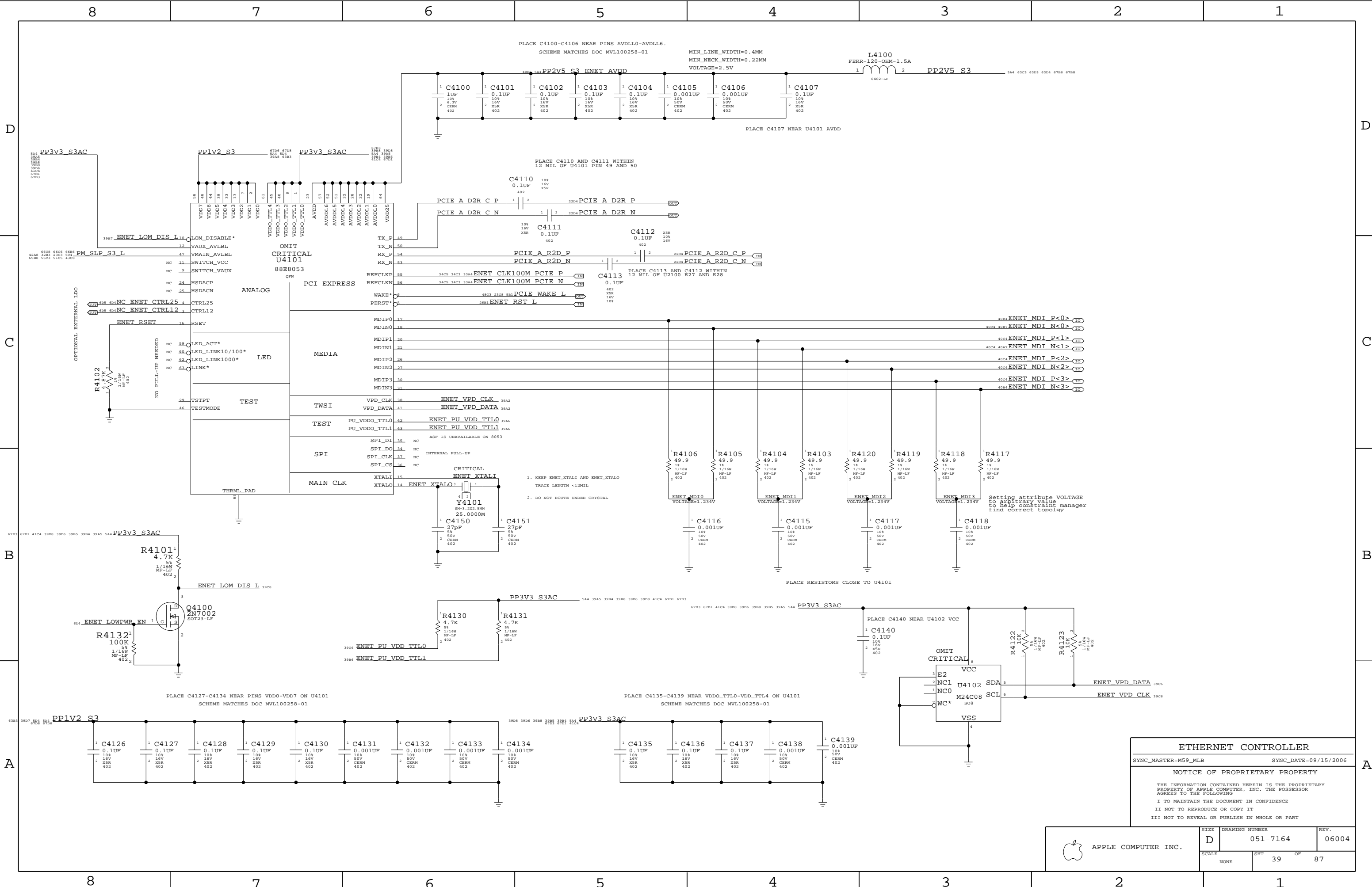
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ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL		
PROVIDED	ENETCONN	ENET_100D	ENETCONN_P<0>	40D3
	ENETCONN	ENET_100D	ENETCONN_N<0>	40C3
	ENETCONN	ENET_100D	ENETCONN_P<1>	40C3
	ENETCONN	ENET_100D	ENETCONN_N<1>	40C3
BY	ENETCONN	ENET_100D	ENETCONN_P<2>	40C3
	ENETCONN	ENET_100D	ENETCONN_N<2>	40C3
	ENETCONN	ENET_100D	ENETCONN_P<3>	40C3
	ENETCONN	ENET_100D	ENETCONN_N<3>	40B3
ETHERNET	ENETCONN	ENET_100D	ENETCONN_P<0>	40D3
PHY	ENETCONN	ENET_100D	ENETCONN_N<0>	40C3
	ENETCONN	ENET_100D	ENETCONN_P<1>	40C3
	ENETCONN	ENET_100D	ENETCONN_N<1>	40C3
	ENETCONN	ENET_100D	ENETCONN_P<2>	40C3

## Page Notes

Power aliases required by this page:

- =PP2V5\_ENET  
- =GND\_CHASSIS\_ENET

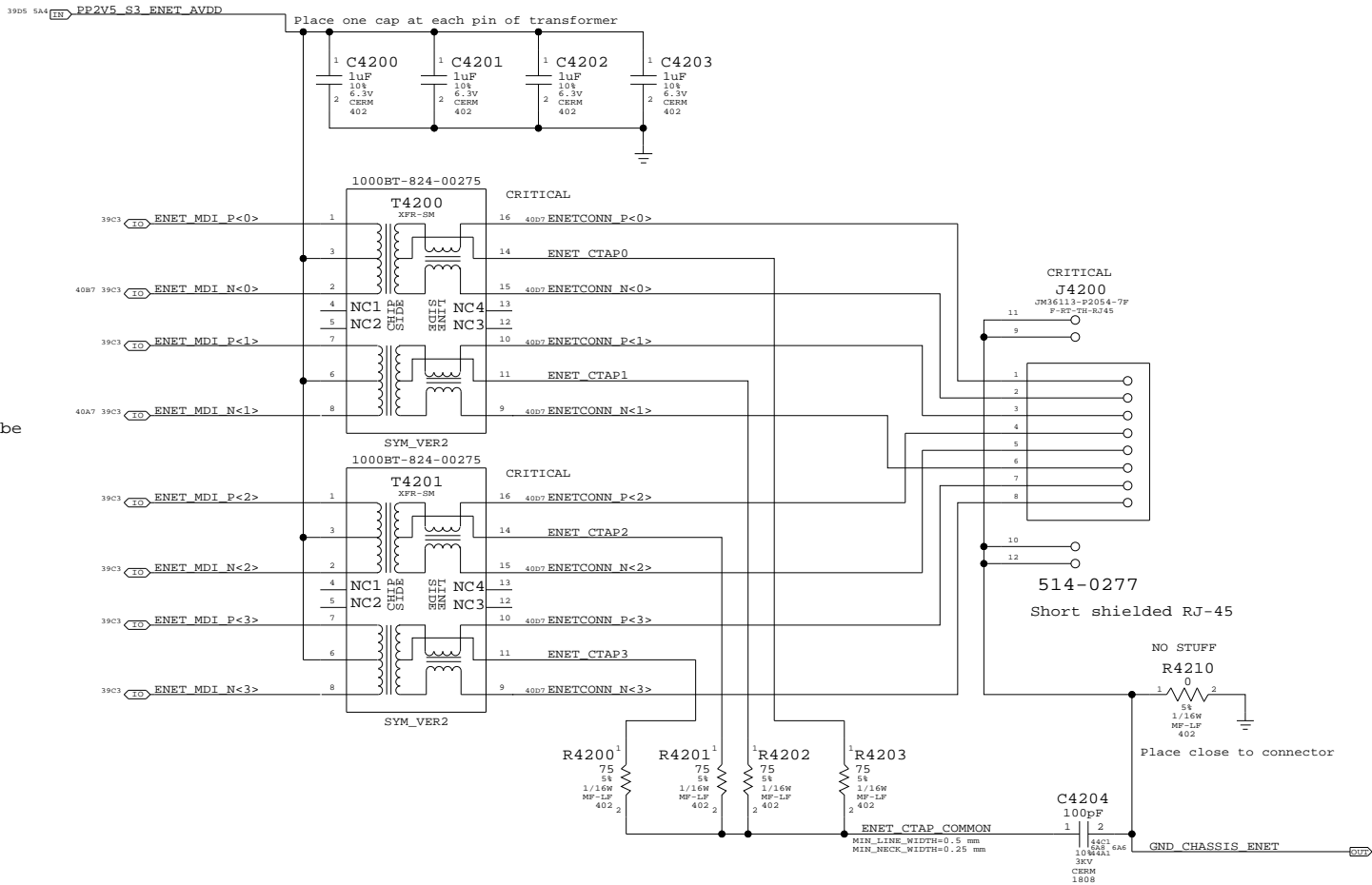
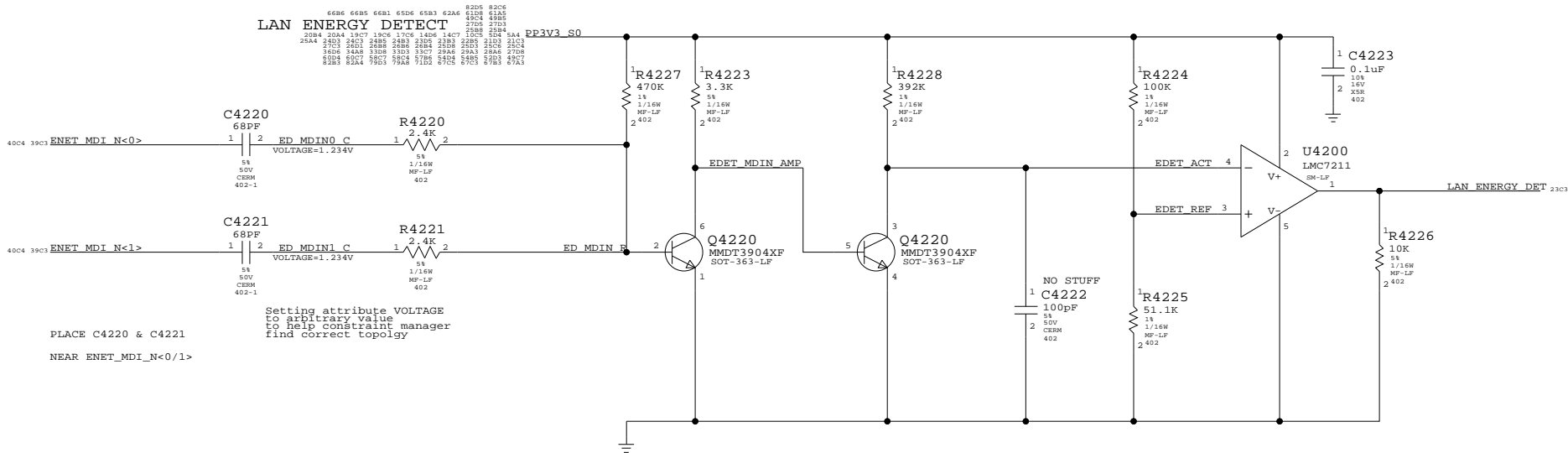
Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

Transformers should be mirrored on opposite sides of the board



## Ethernet Connector

SYNC\_MASTER=M59\_MLB SYNC\_DATE=09/15/2006

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D	051-7164	06004
SCALE	SHT	OF
NONE	40	87



D

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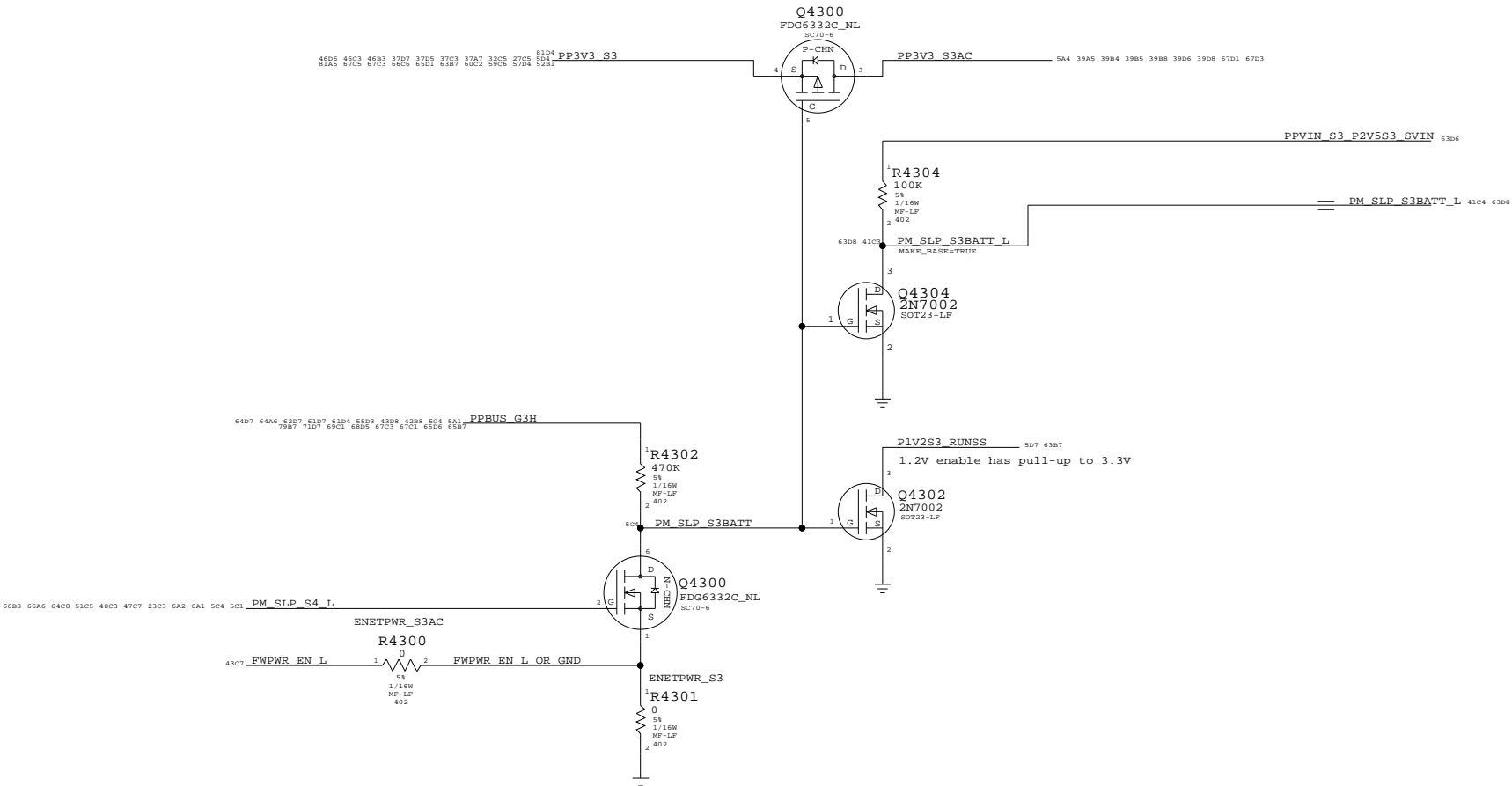
C

B

A

# Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR\_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

When ENETPWR\_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

## Yukon Power Control

SYNC\_MASTER=M59\_MLB

SYNC\_DATE=09/15/2006

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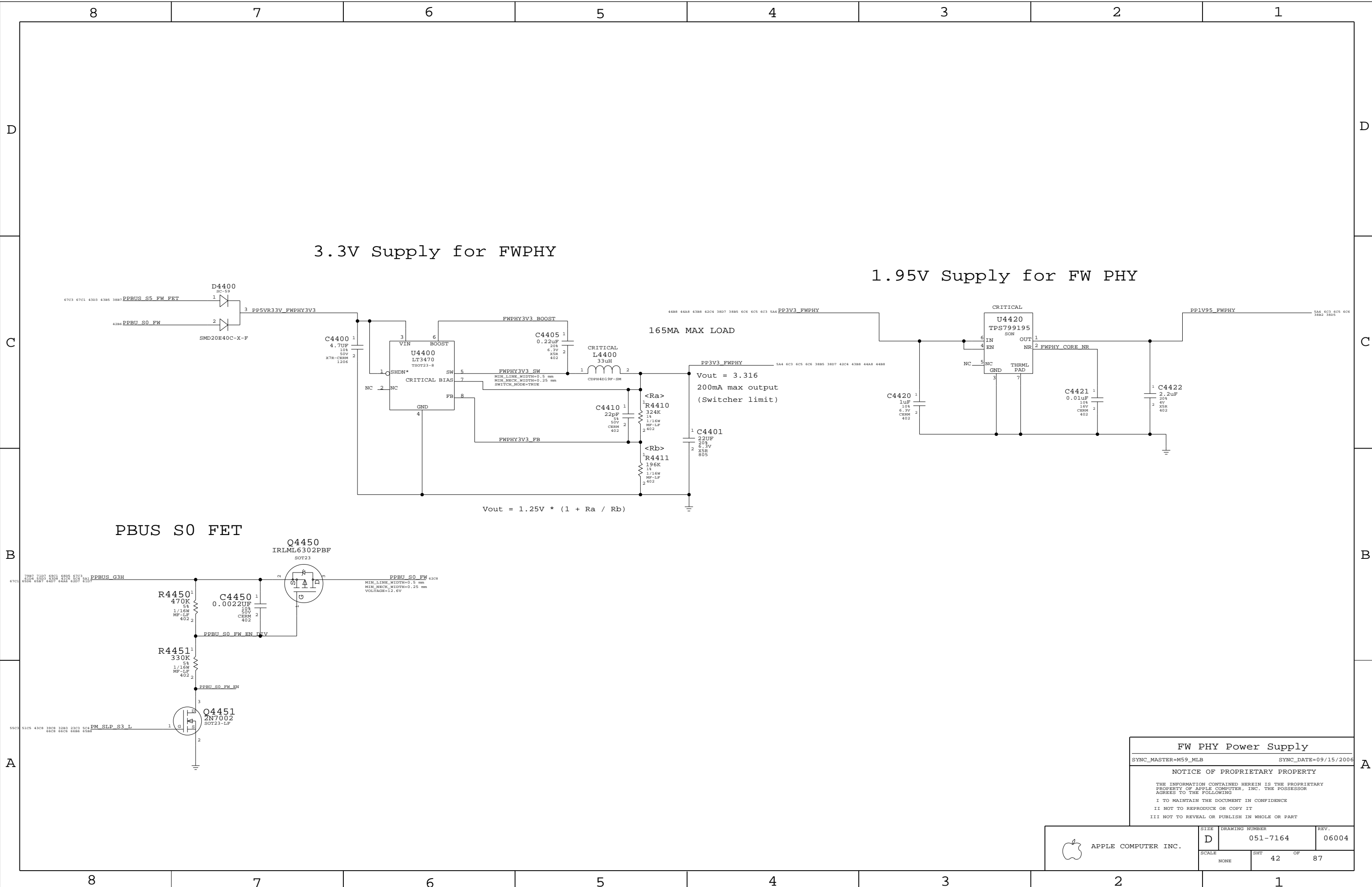
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SHT

41

OF

87



FW PHY Power Supply

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	SCALE NONE	SHT 42	OF 87

## Page Notes

Power aliases required by this page:

- =PPBUS\_S0\_FWPWRSW (system supply for bus power)
- =PP3V3\_S0\_FWPORTPWRSW

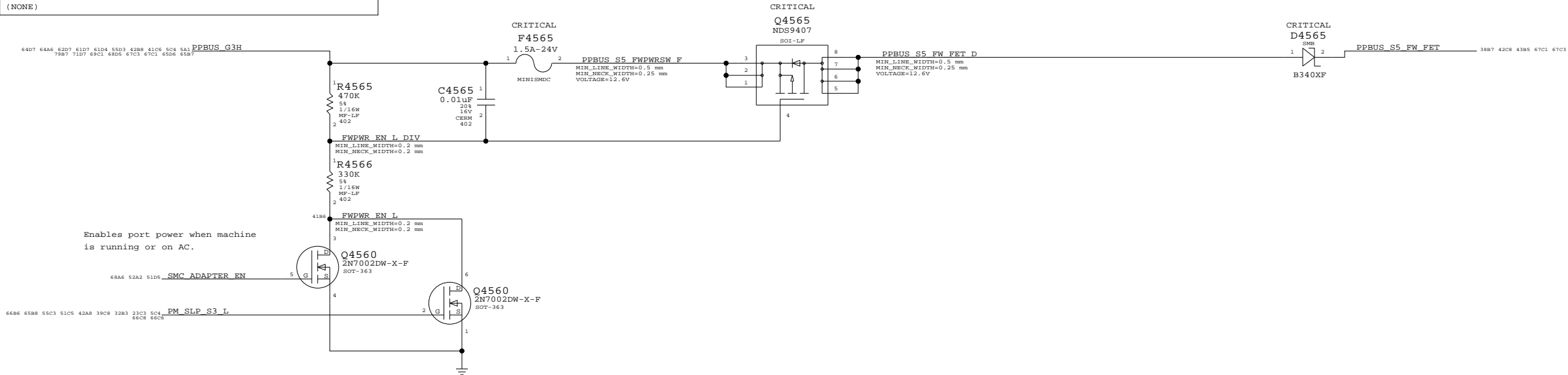
Signal aliases required by this page:

- =FWPWR\_PWRON (see related text note below)

BOM options provided by this page:

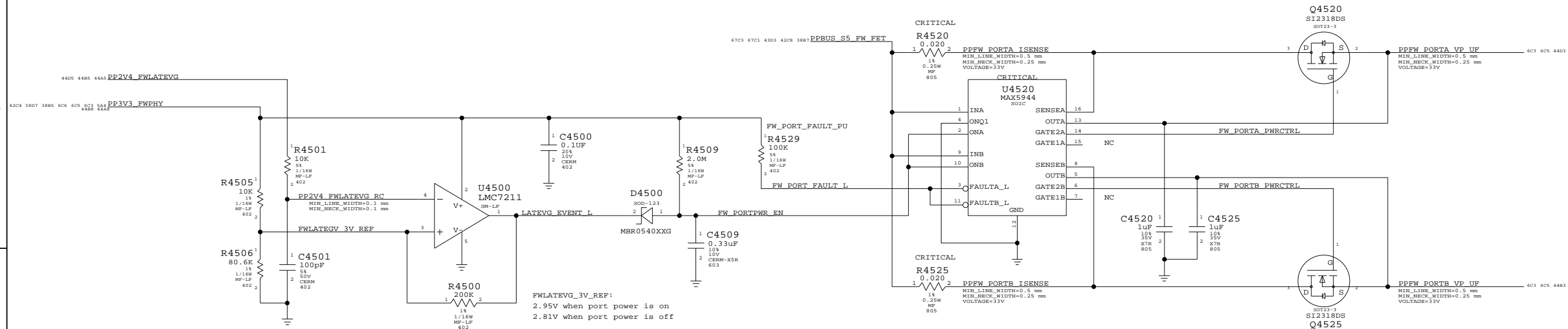
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### Port Power Switch



### Current Limit/Active Late-VG Protection

#### Late-VG Event Detection



#### Current Limits

0.020 ohm => 2.4A  
0.025 ohm => 2A  
0.030 ohm => 1.66A (Ideal)  
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

### FireWire Port Power

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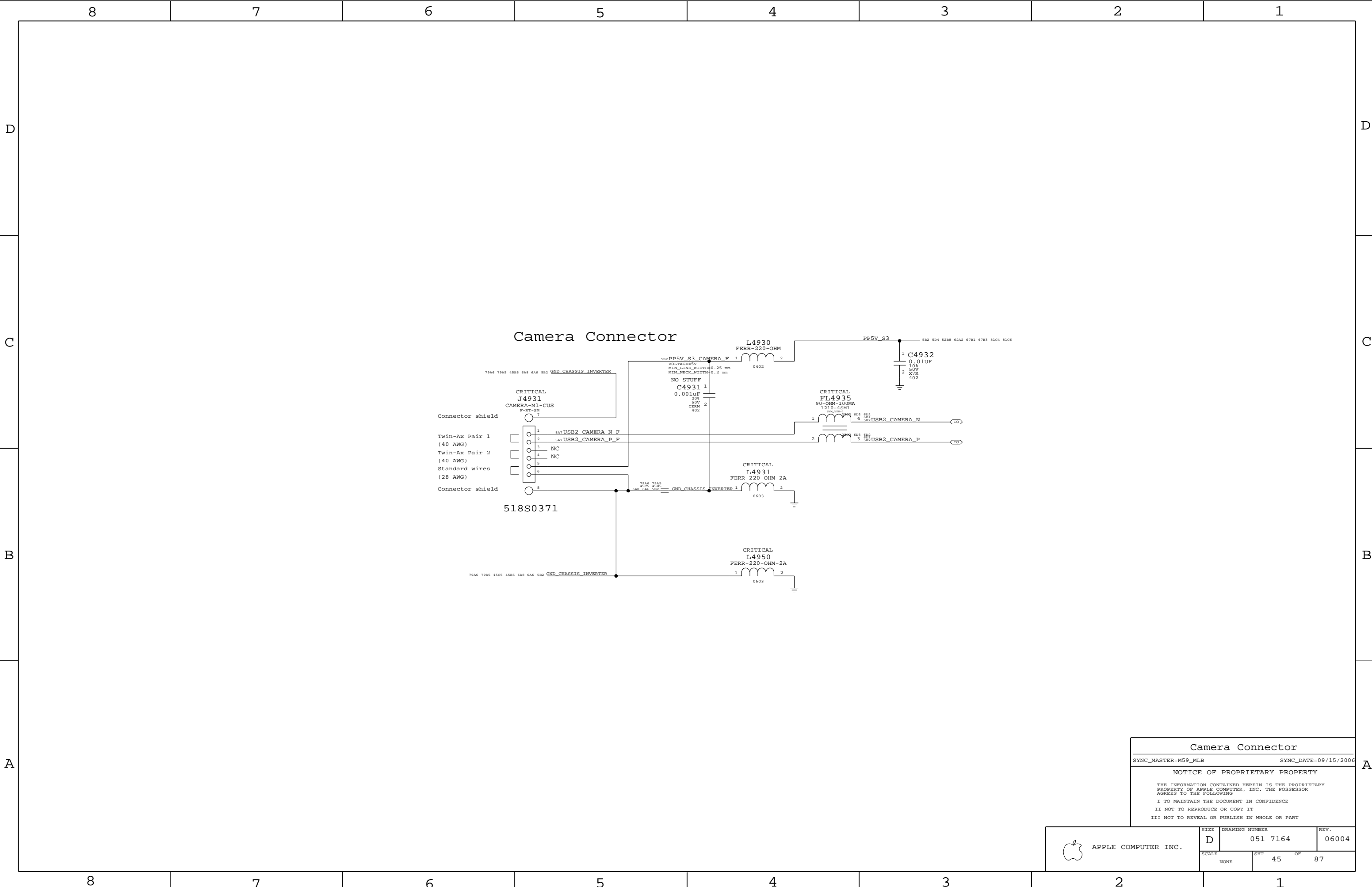
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SCALE	SHT	OF
NONE	43	87





Camera Connector

SYNC\_MASTER=M59\_MLB SYNC\_DATE=09/15/2006

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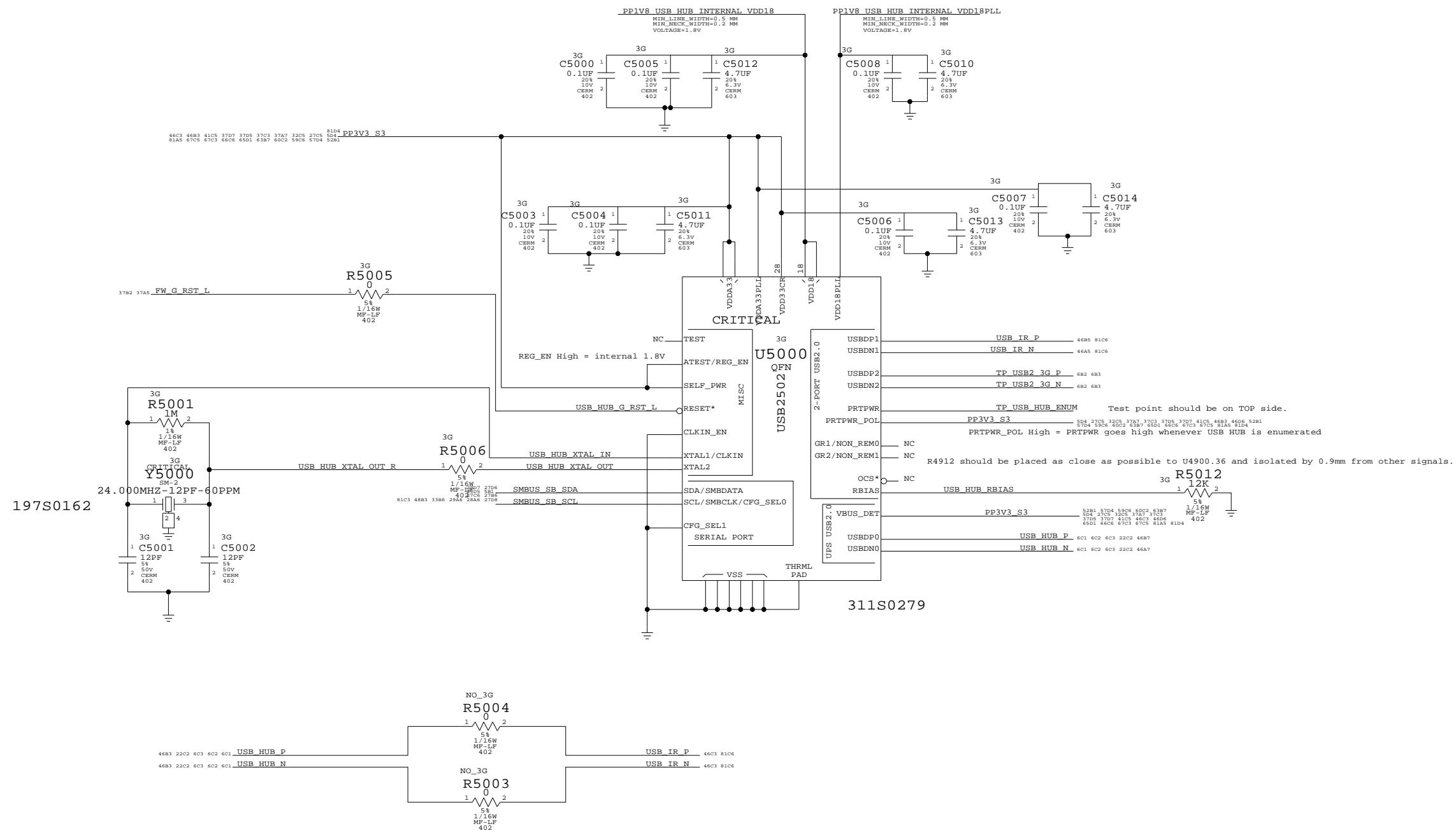
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## Internal USB Hub

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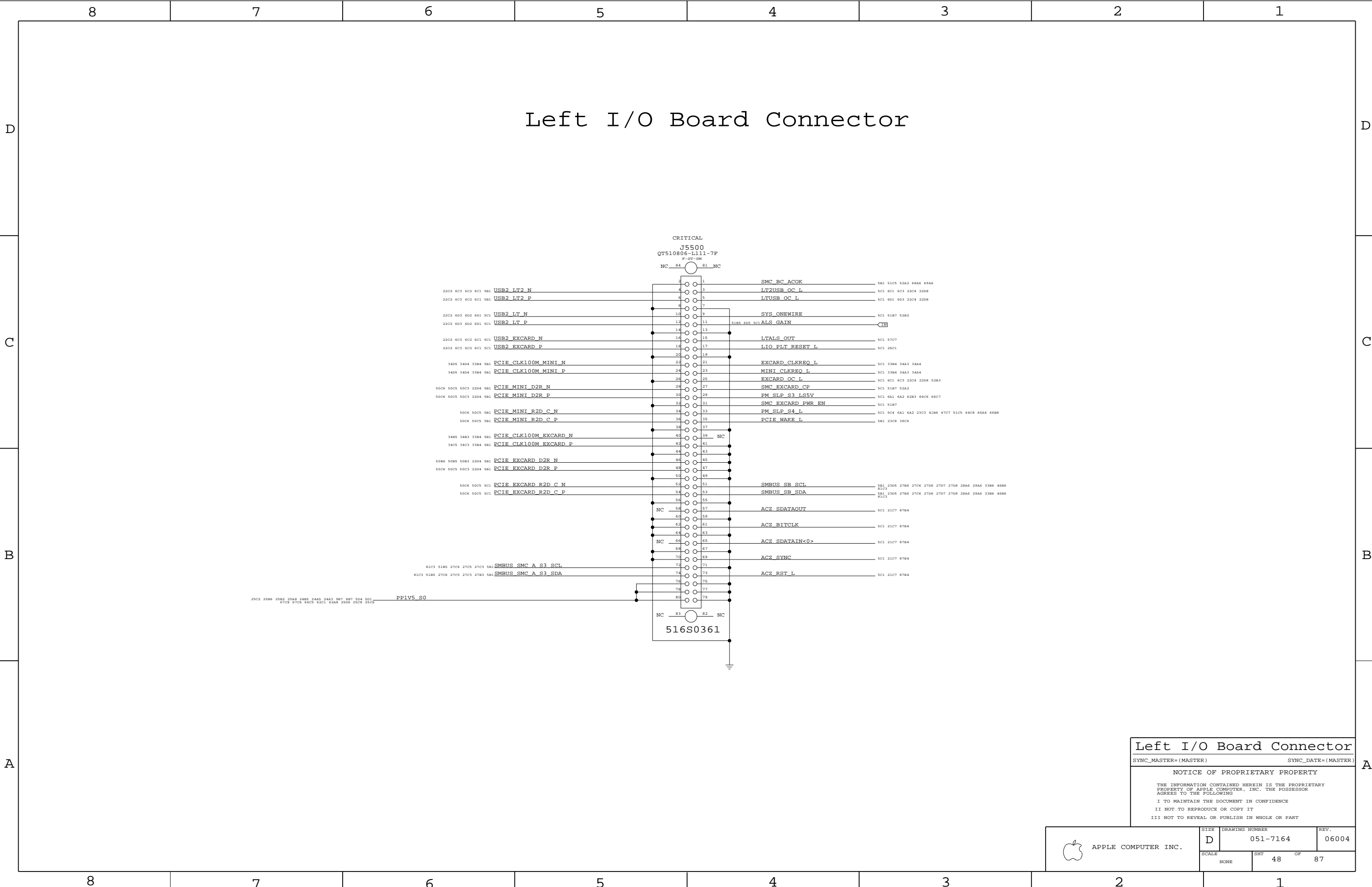
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Left I/O Board Connector

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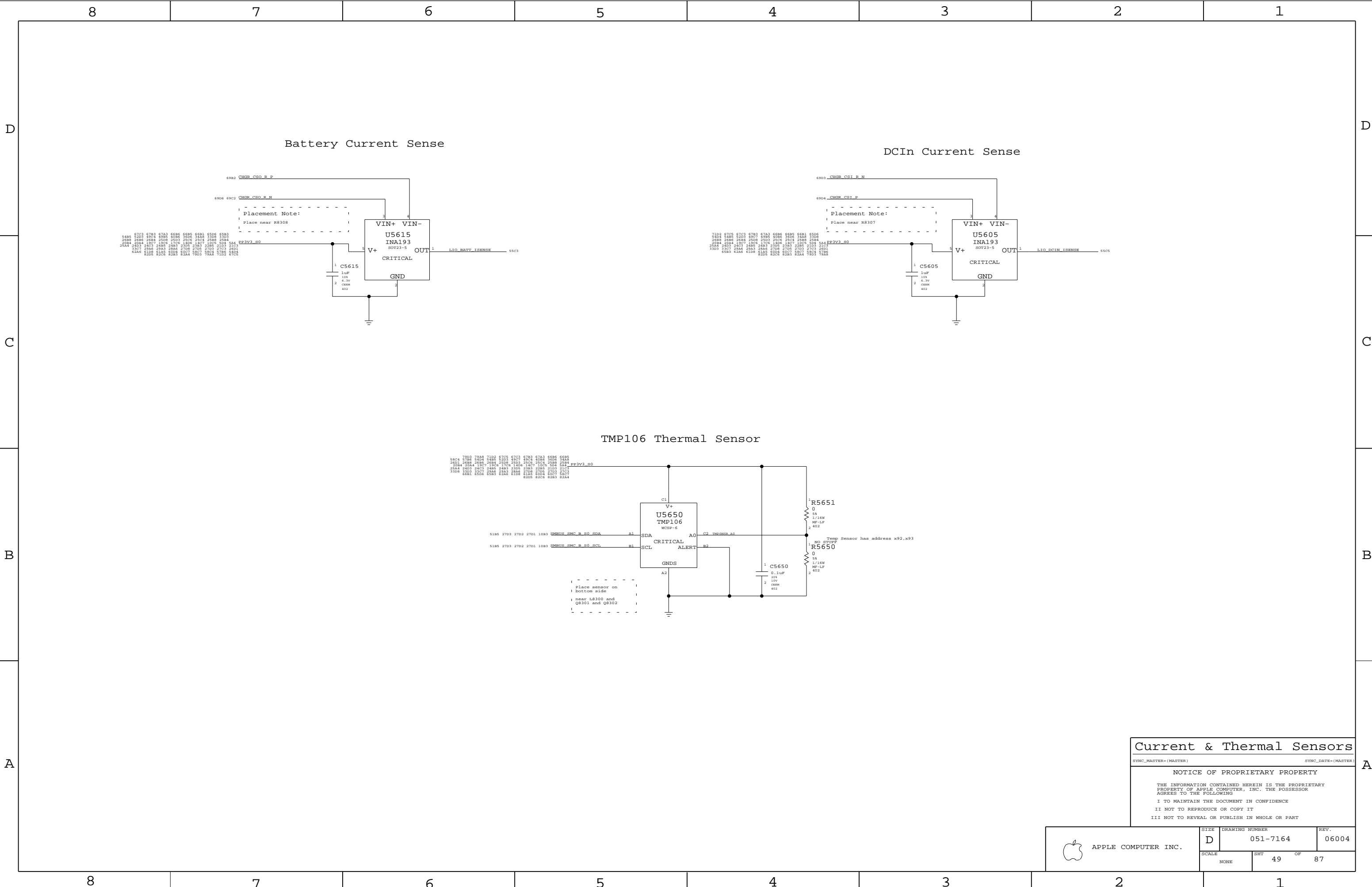
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NONE	48	87





# Current & Thermal Sensors

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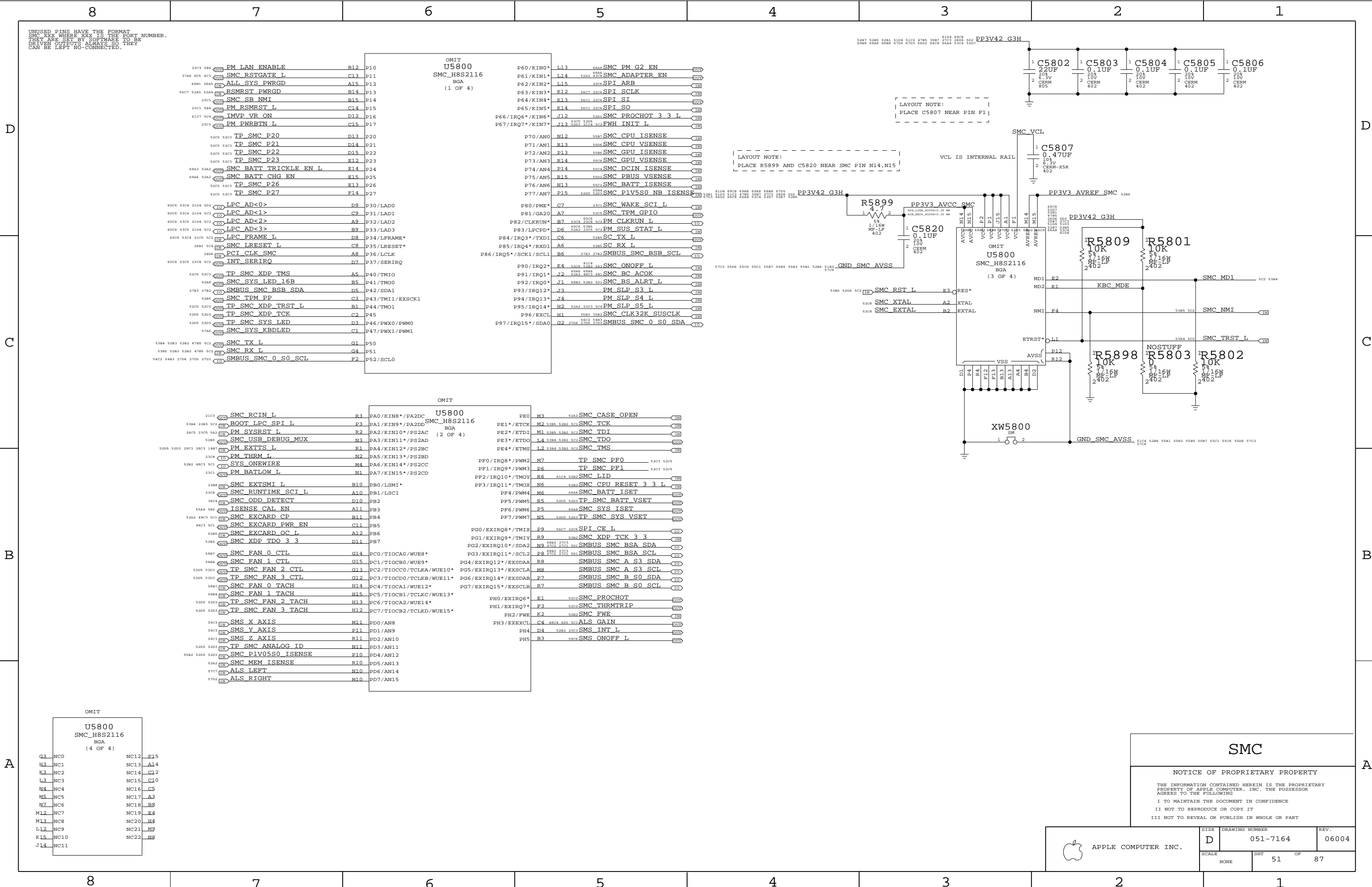
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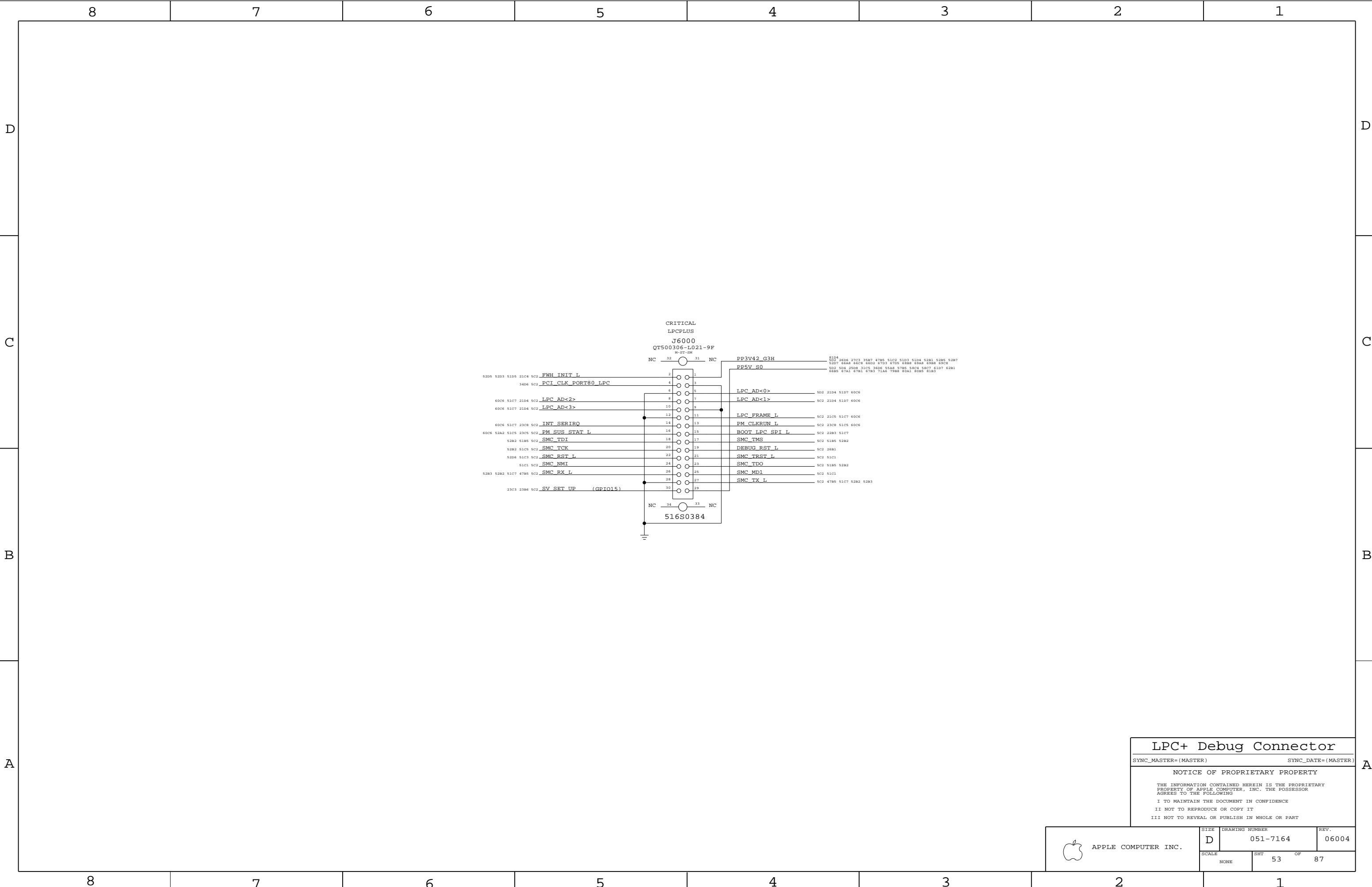
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SIZE	DRAWING NUMBER	REV.
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NONE	49	87









LPC+ Debug Connector

SYNC\_MASTER=(MASTER)SYNC\_DATE=(MASTER)


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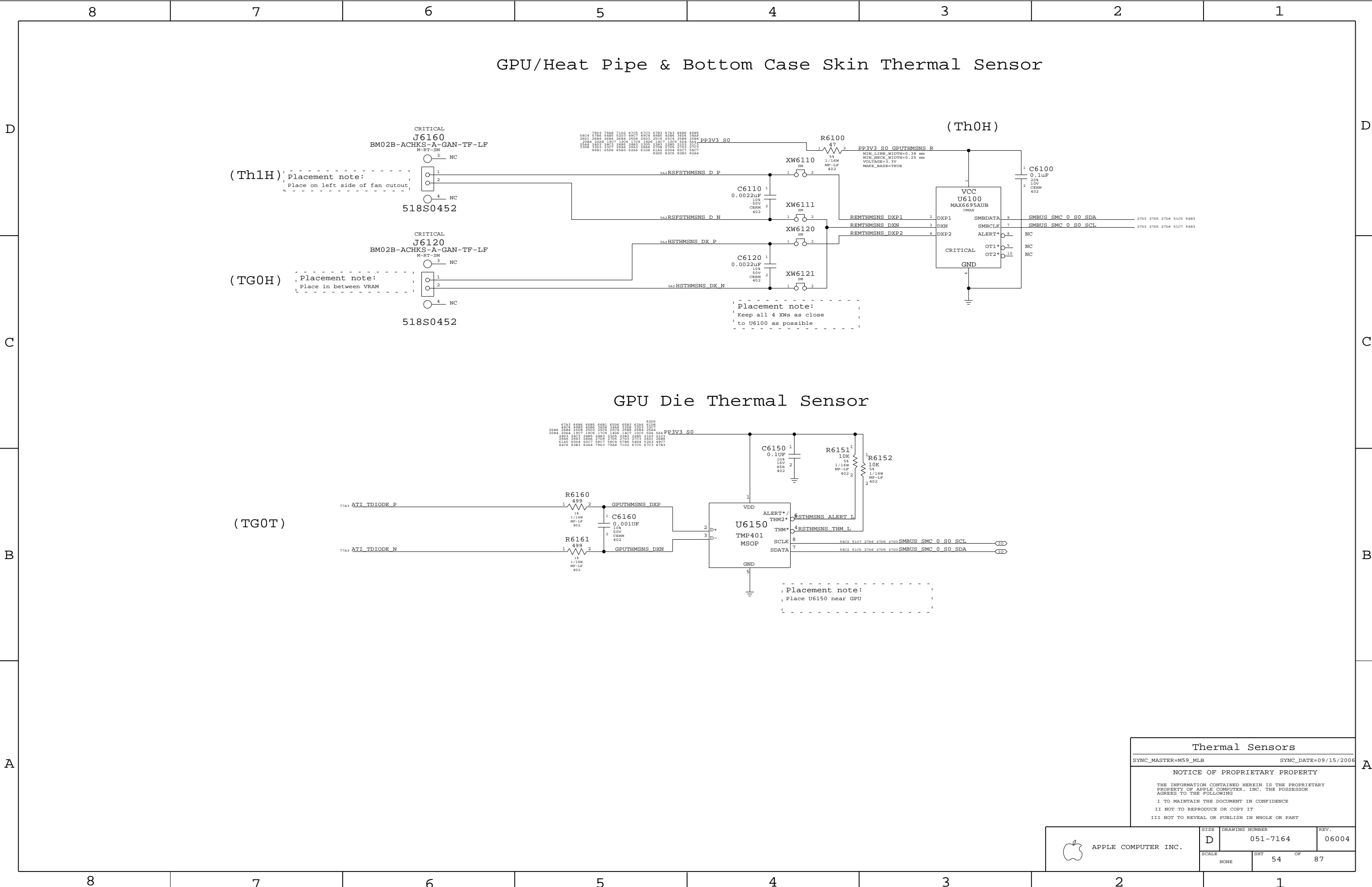
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Thermal Sensors

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SYNC\_DATE=09/15/2006

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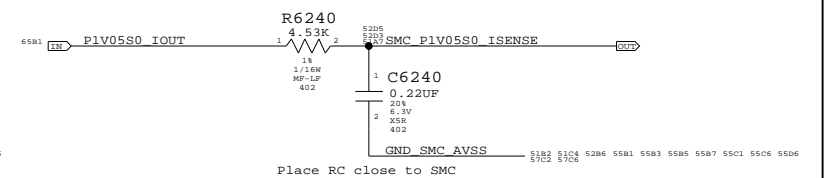
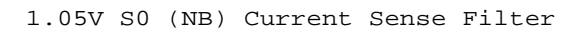
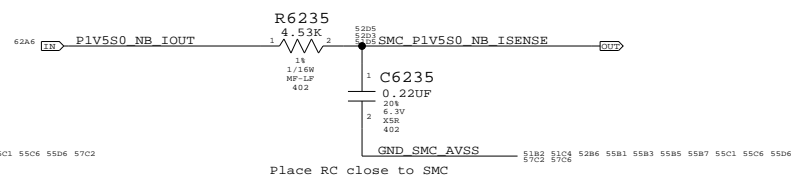
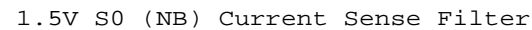
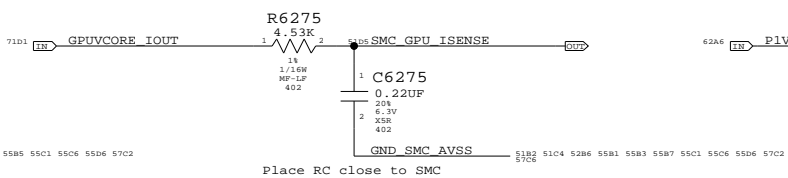
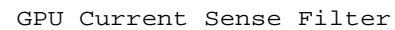
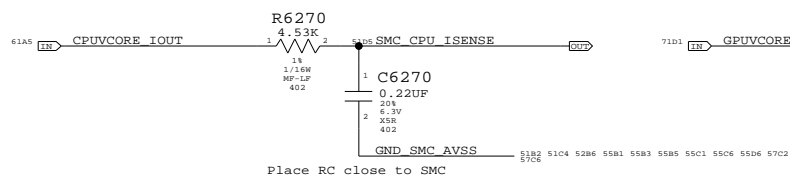
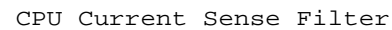
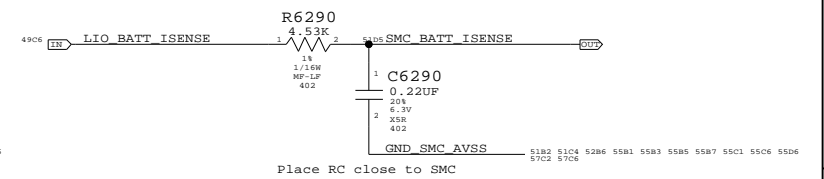
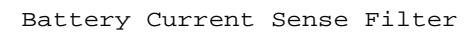
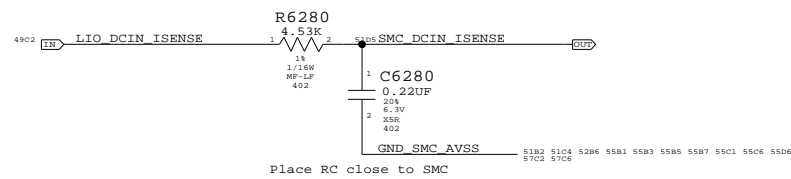
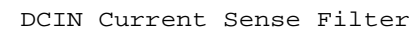
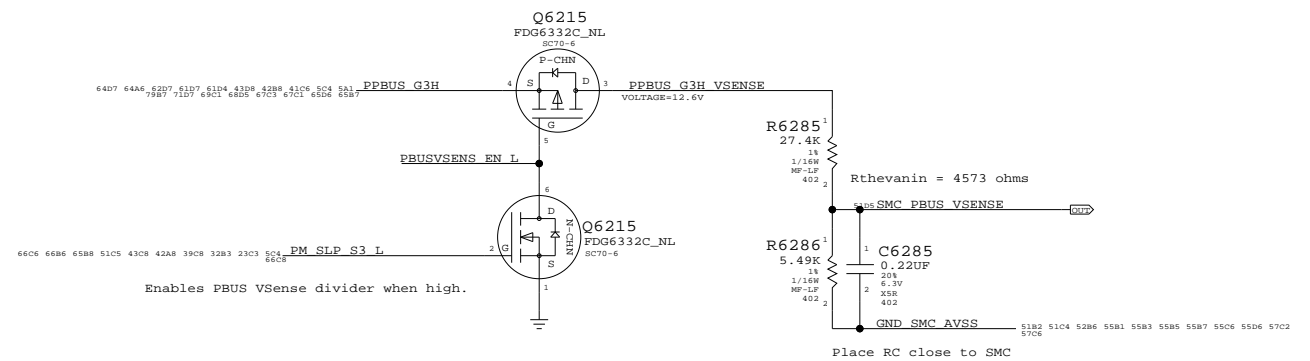
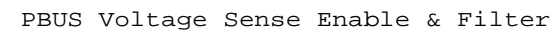
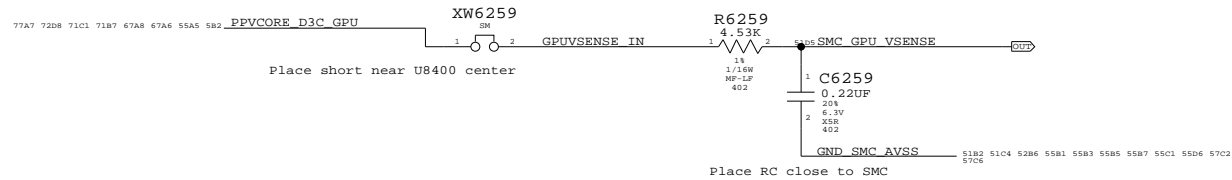
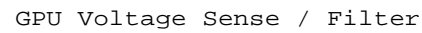
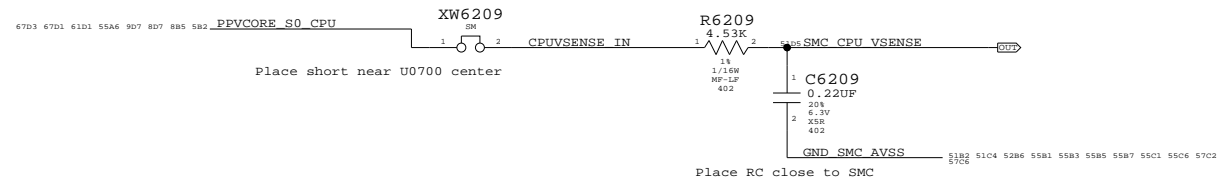
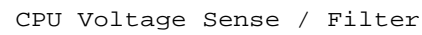
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54

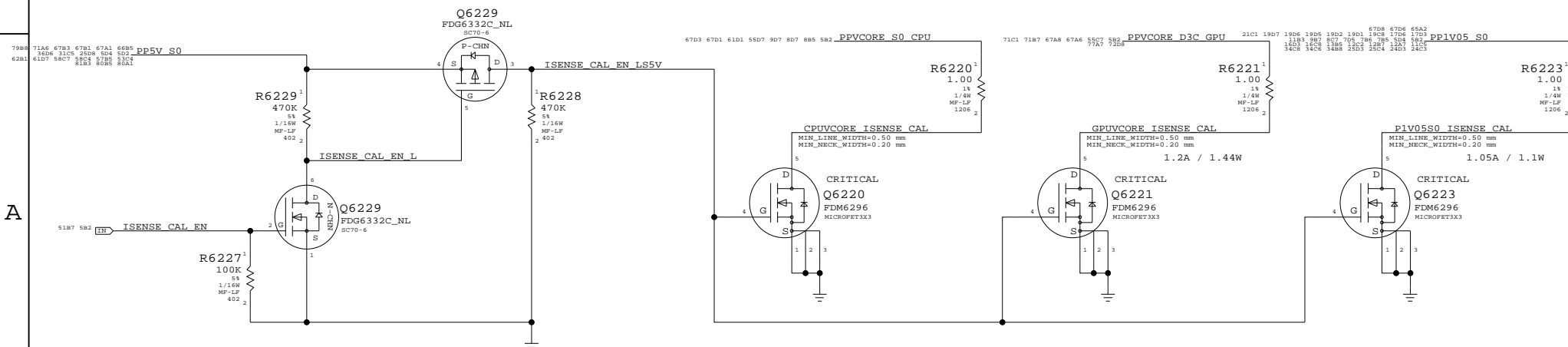
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87




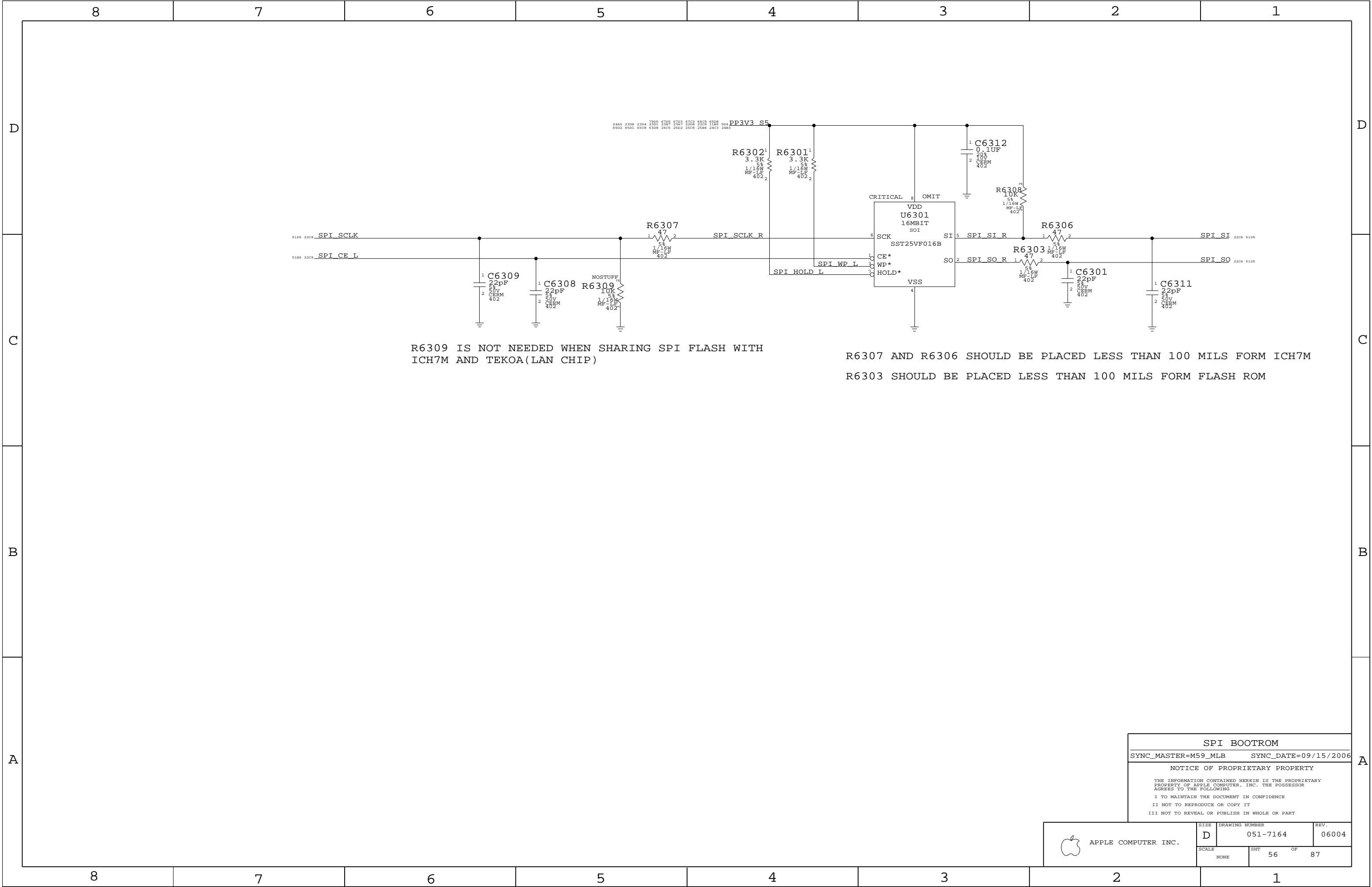
## Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing	
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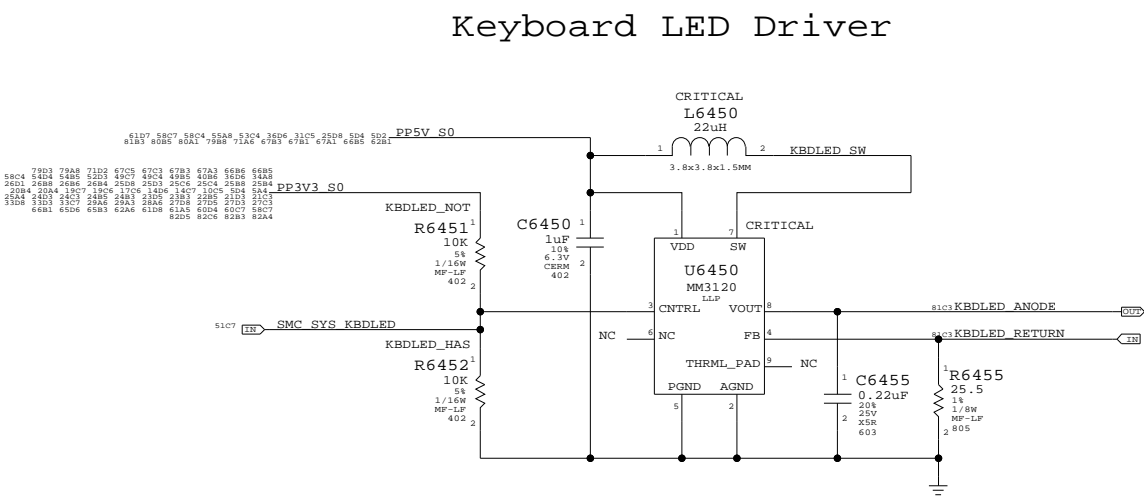
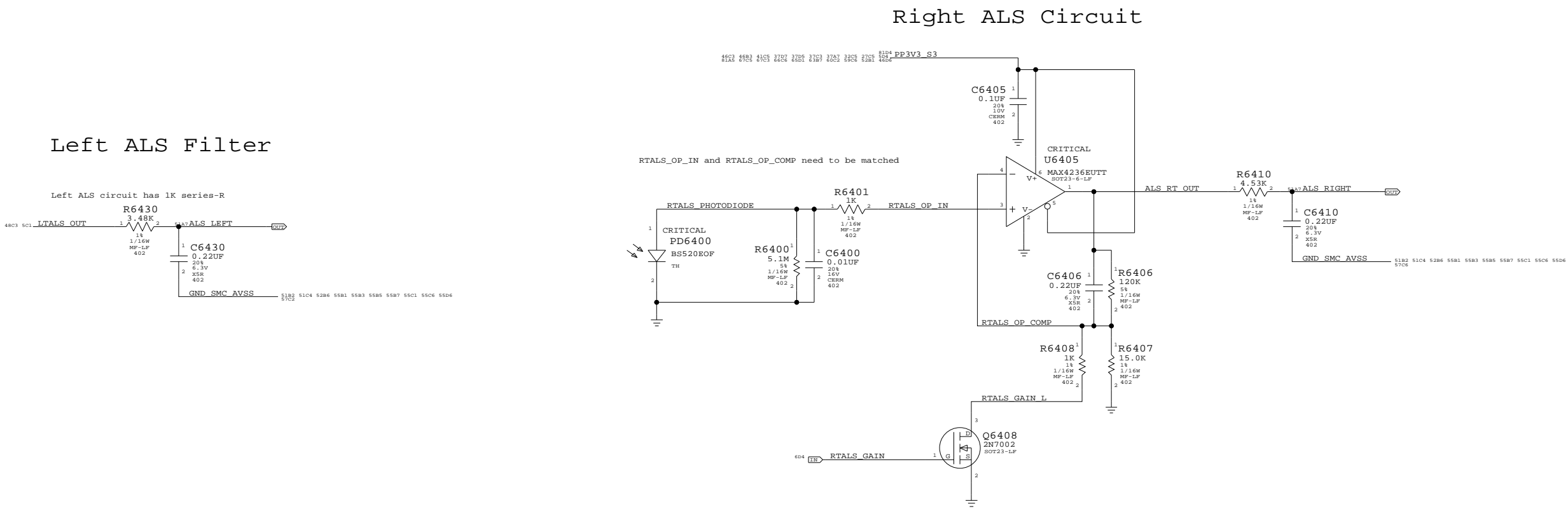
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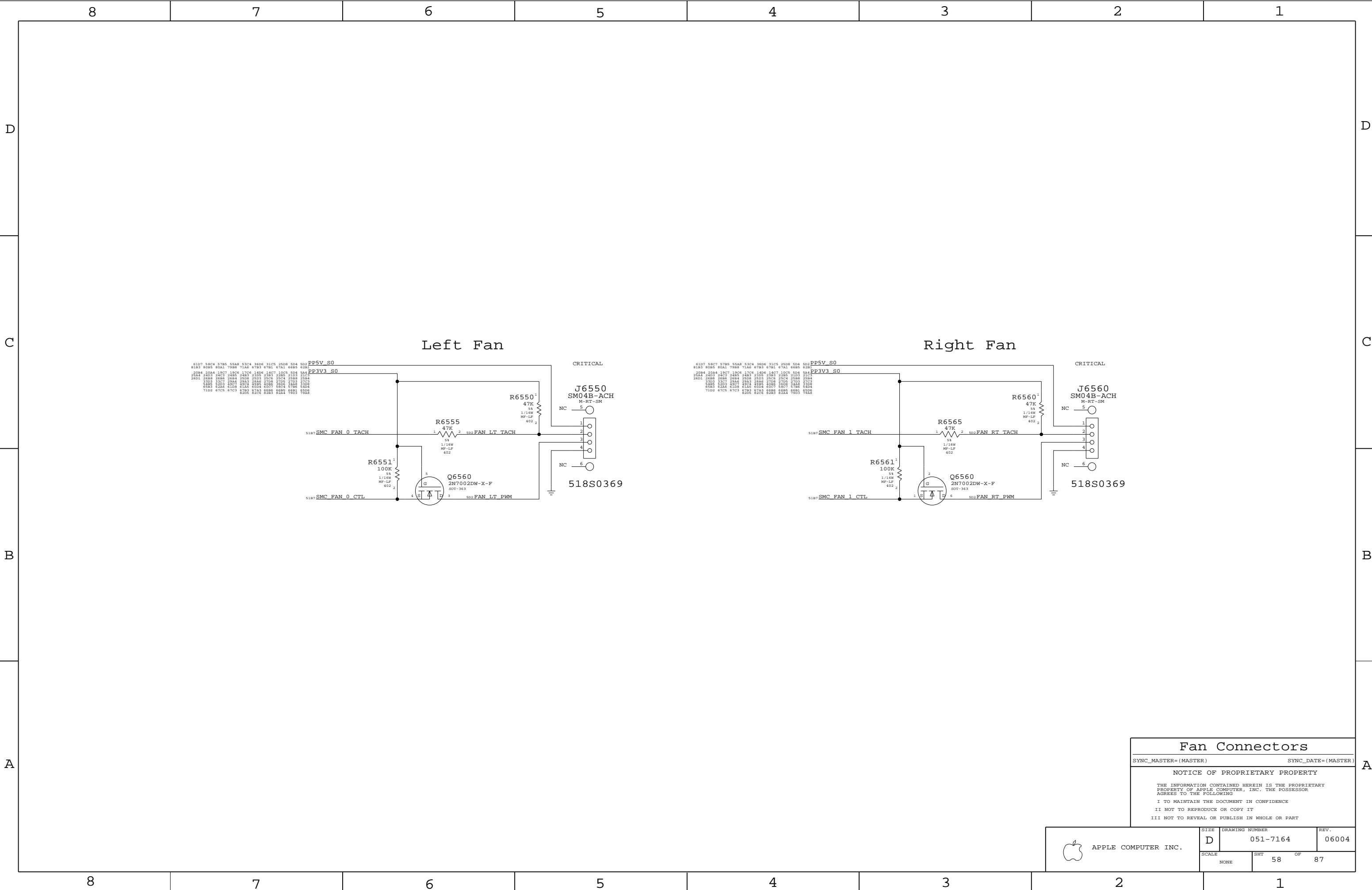
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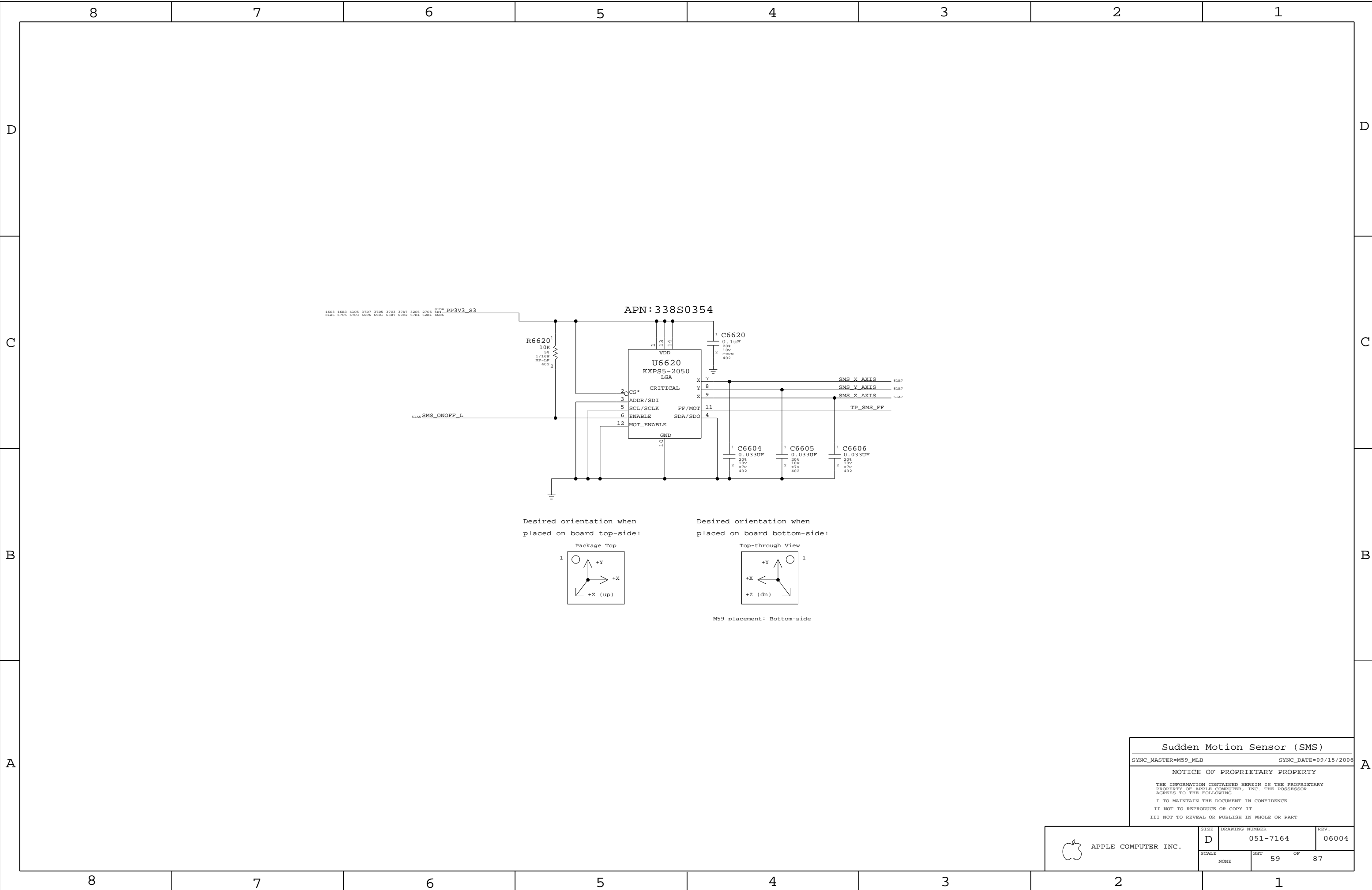
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ALS Support		
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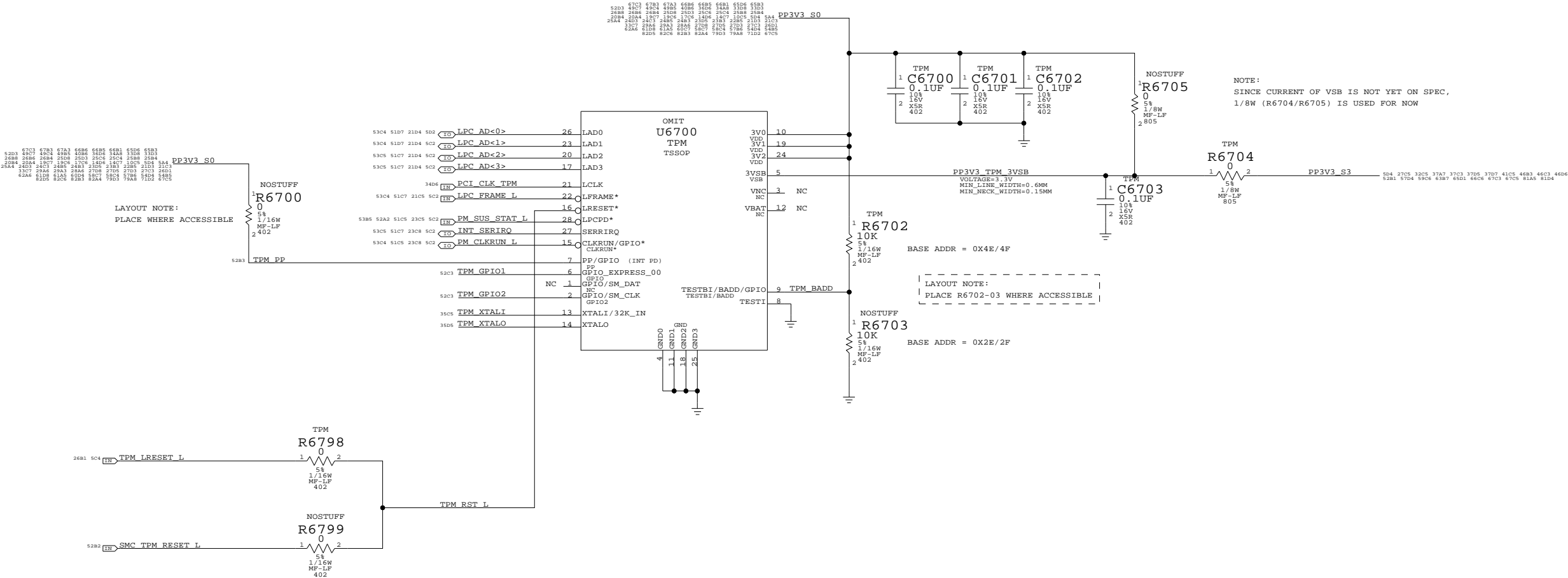
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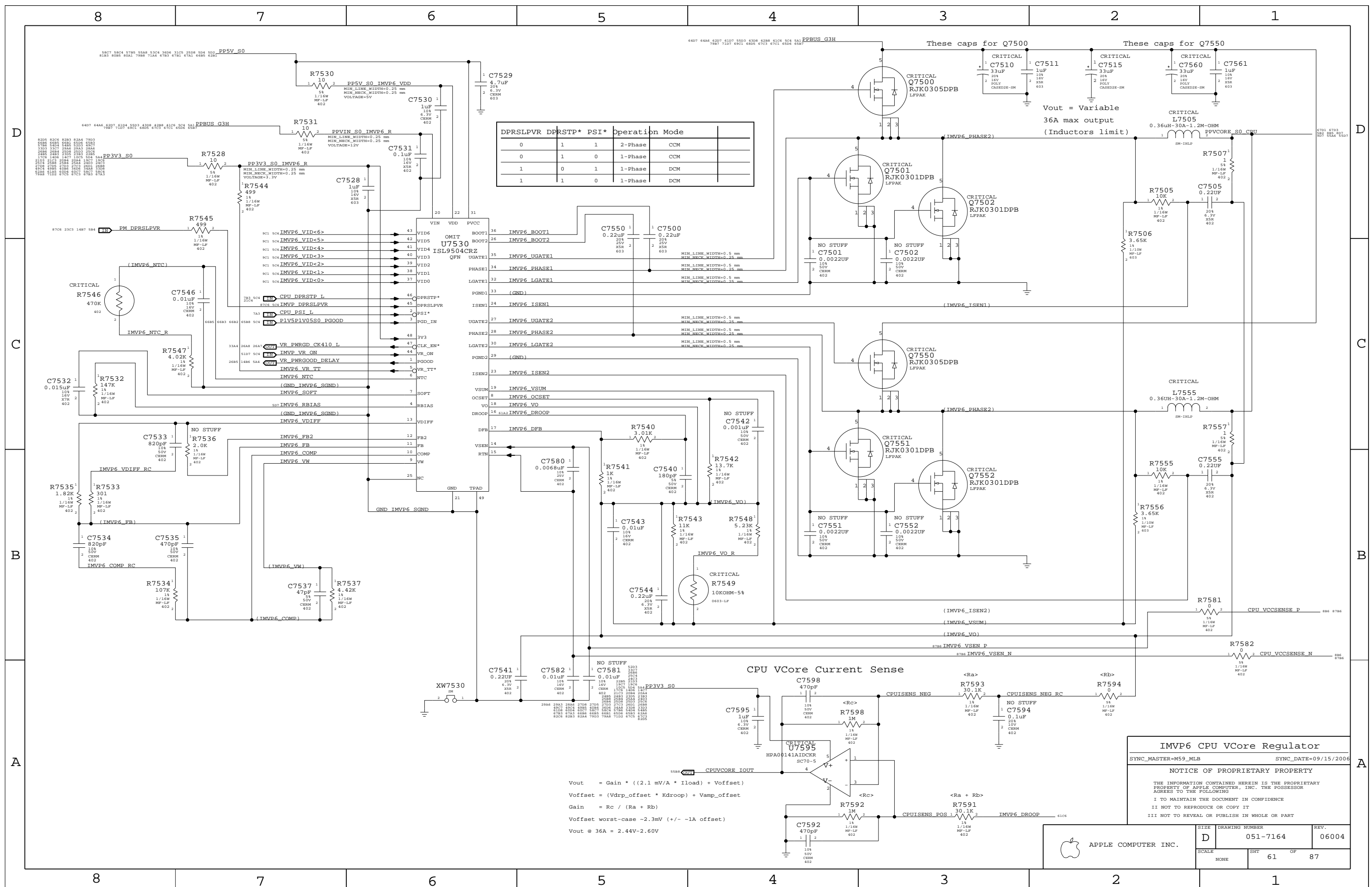
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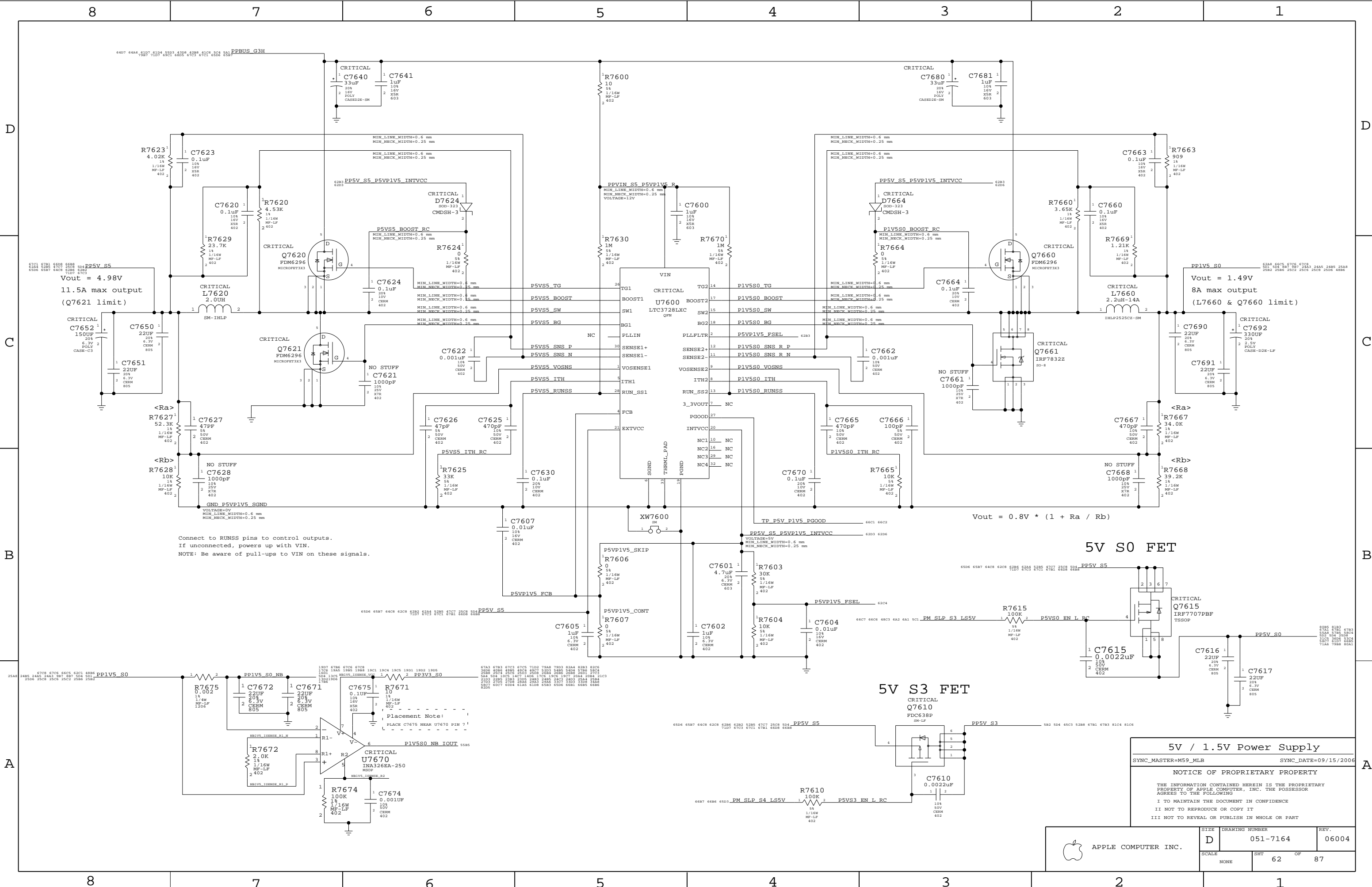
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TPM		
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5V / 1.5V Power Supply

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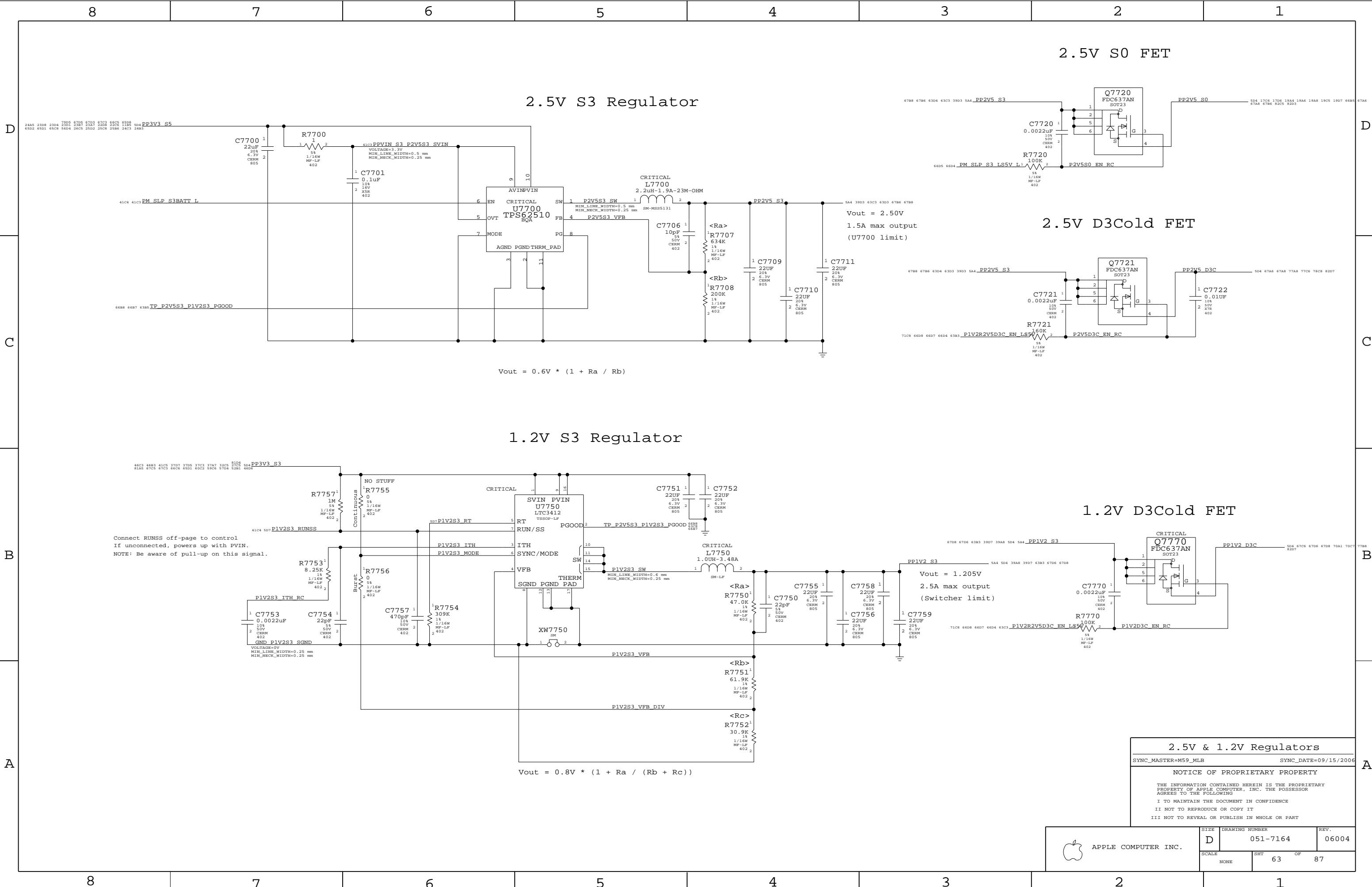
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NONE		62	87



2.5V S3 Regulator

2.5V S0 FET

2.5V D3Cold FET

1.2V S3 Regulator

1.2V D3Cold FET

2.5V & 1.2V Regulators

SYNC\_MASTER=M59\_MLB SYNC\_DATE=09/15/2006

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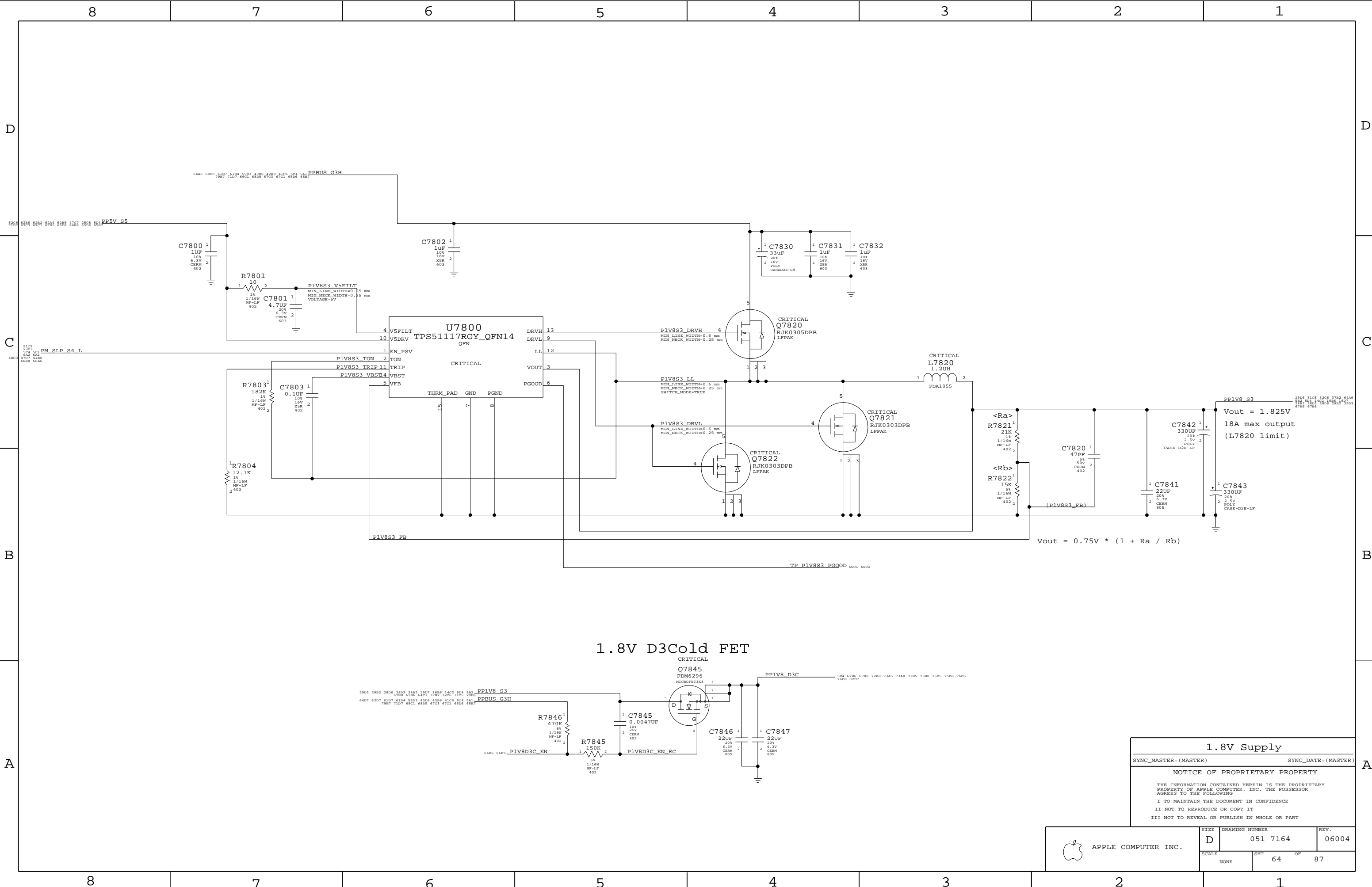
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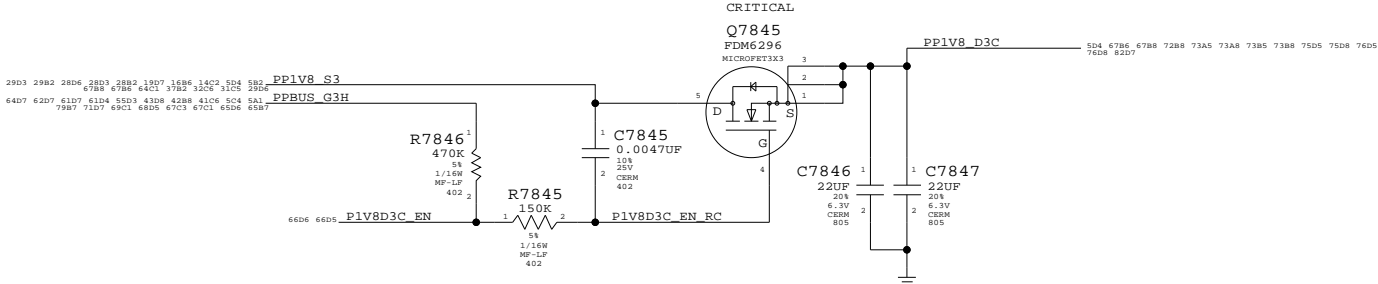
63

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1.8V D3Cold FET



1.8V Supply

SYNC\_MASTER=(MASTER)

SYNC\_DATE=(MASTER)

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SCALE		SHT	OF
NONE		64	87









## D



## C



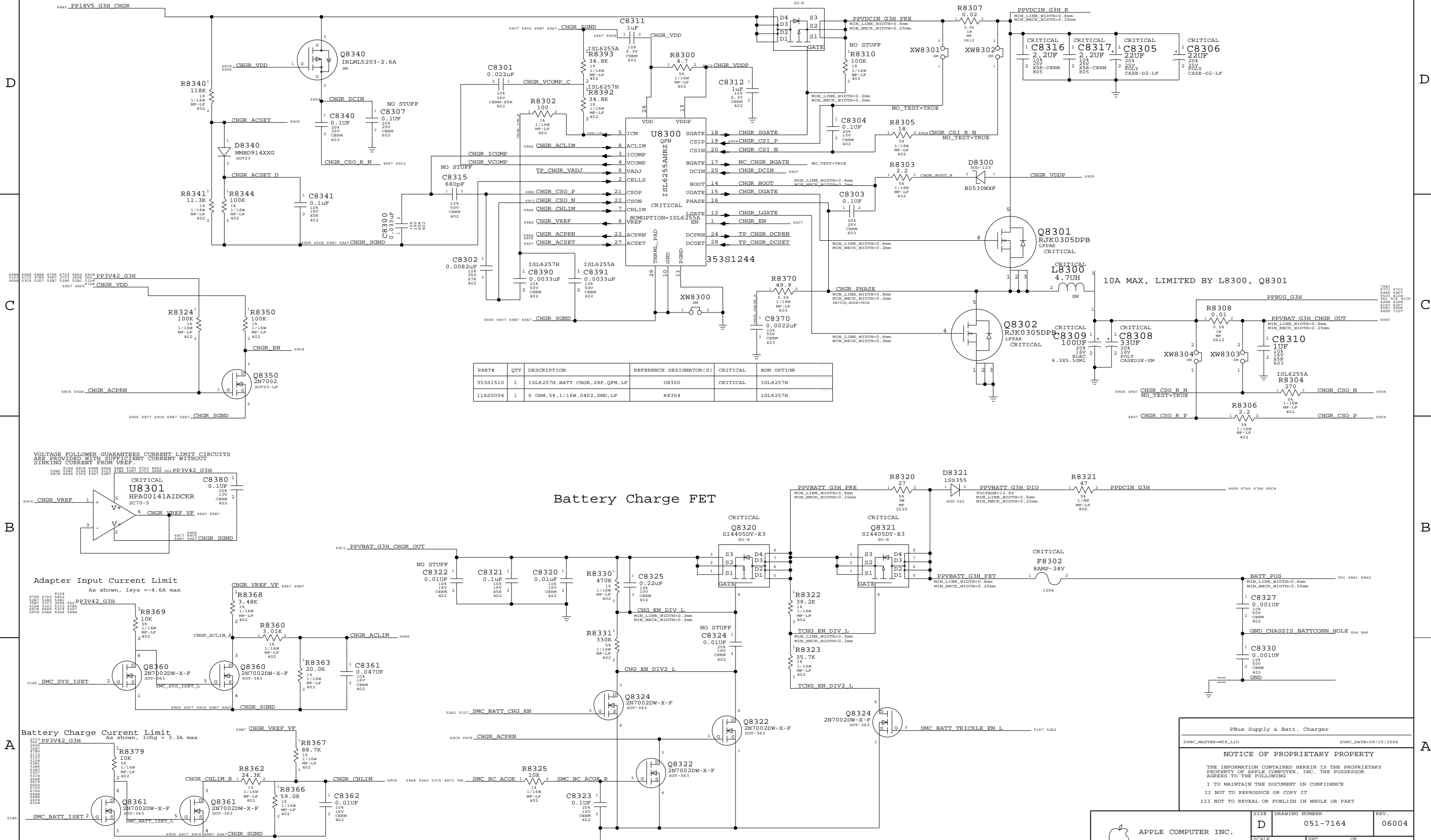
## B



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SIZE D	DRAWING NUMBER 051-7164	REV. 06004
SCALE NONE	SHT 68	OF 87

PBus Supply & Battery Charger



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1510	1	ISL6257H, BATT CHGR, 28P, QFN, LF	U8300	CRITICAL	ISL6257H
116S0004	1	0 OHM, 5%, 1/16W, 0402, SMD, LF	R8304		ISL6257H

Battery Charge FET

PBus Supply & Batt. Charger

SYNC\_MASTER=M59\_L10 SYNC\_DATE=09/15/2006

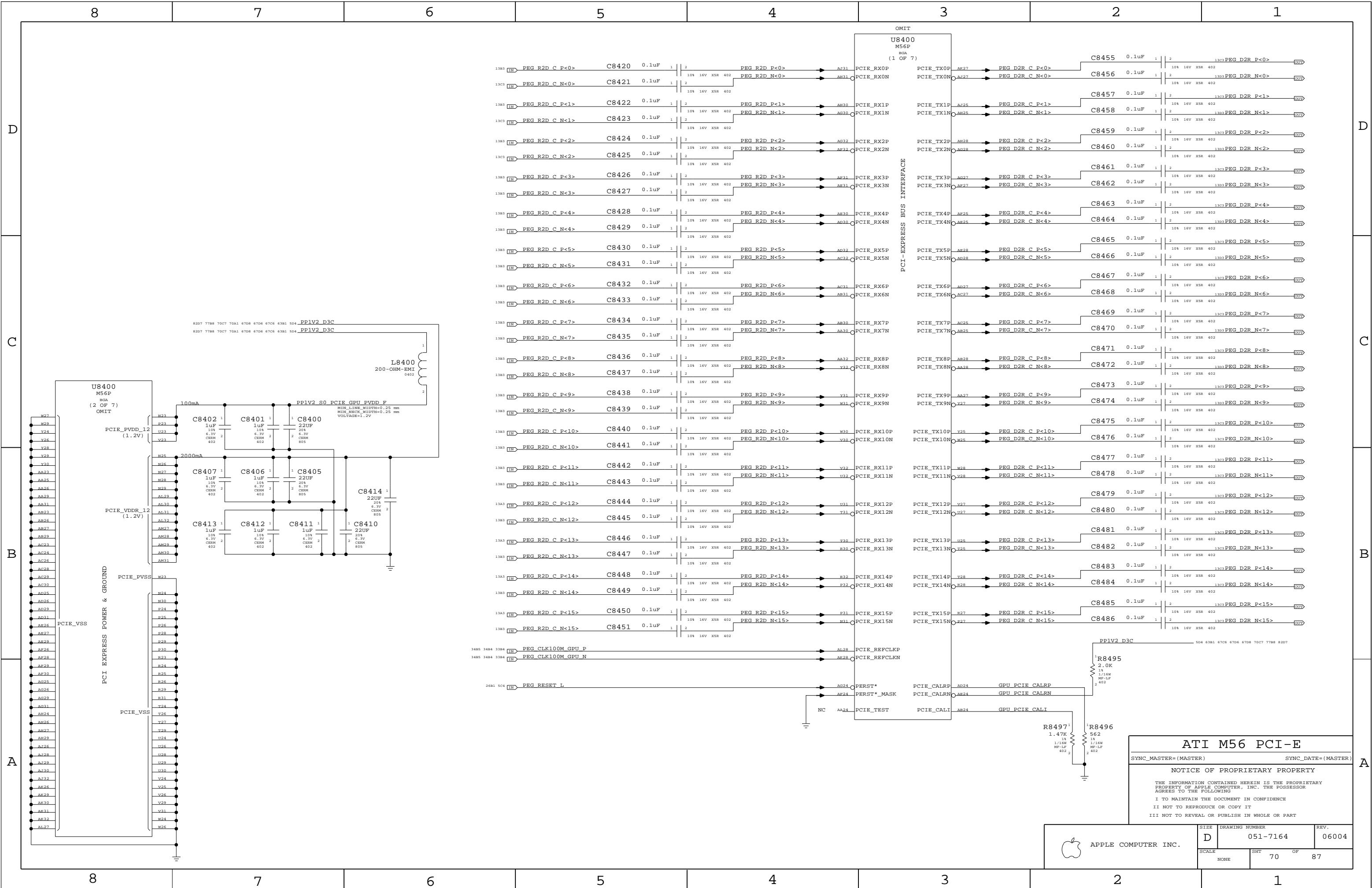
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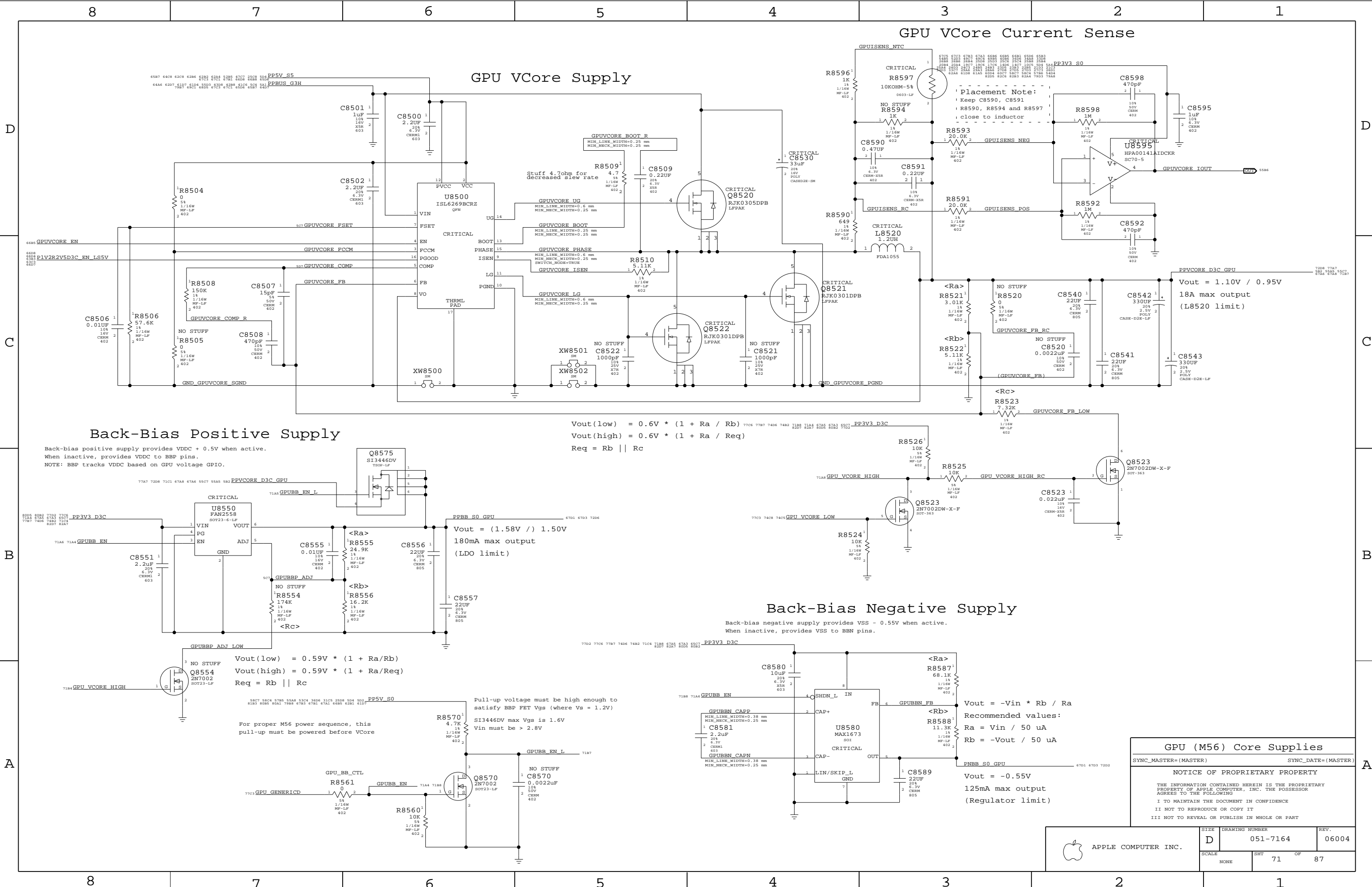
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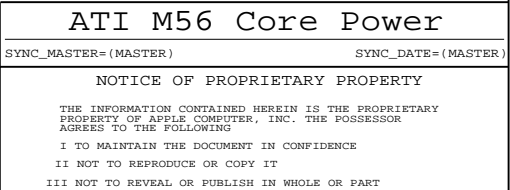
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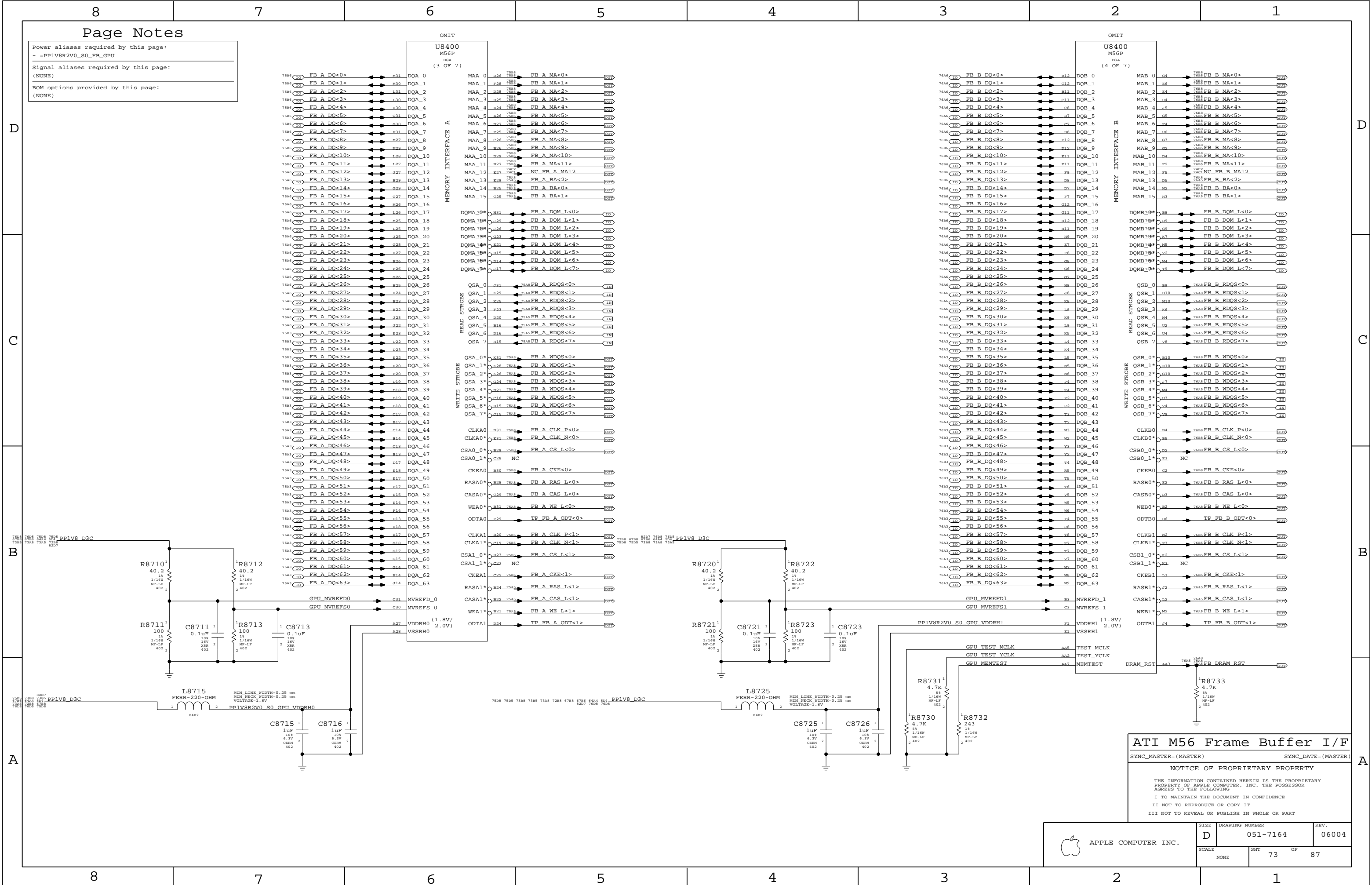


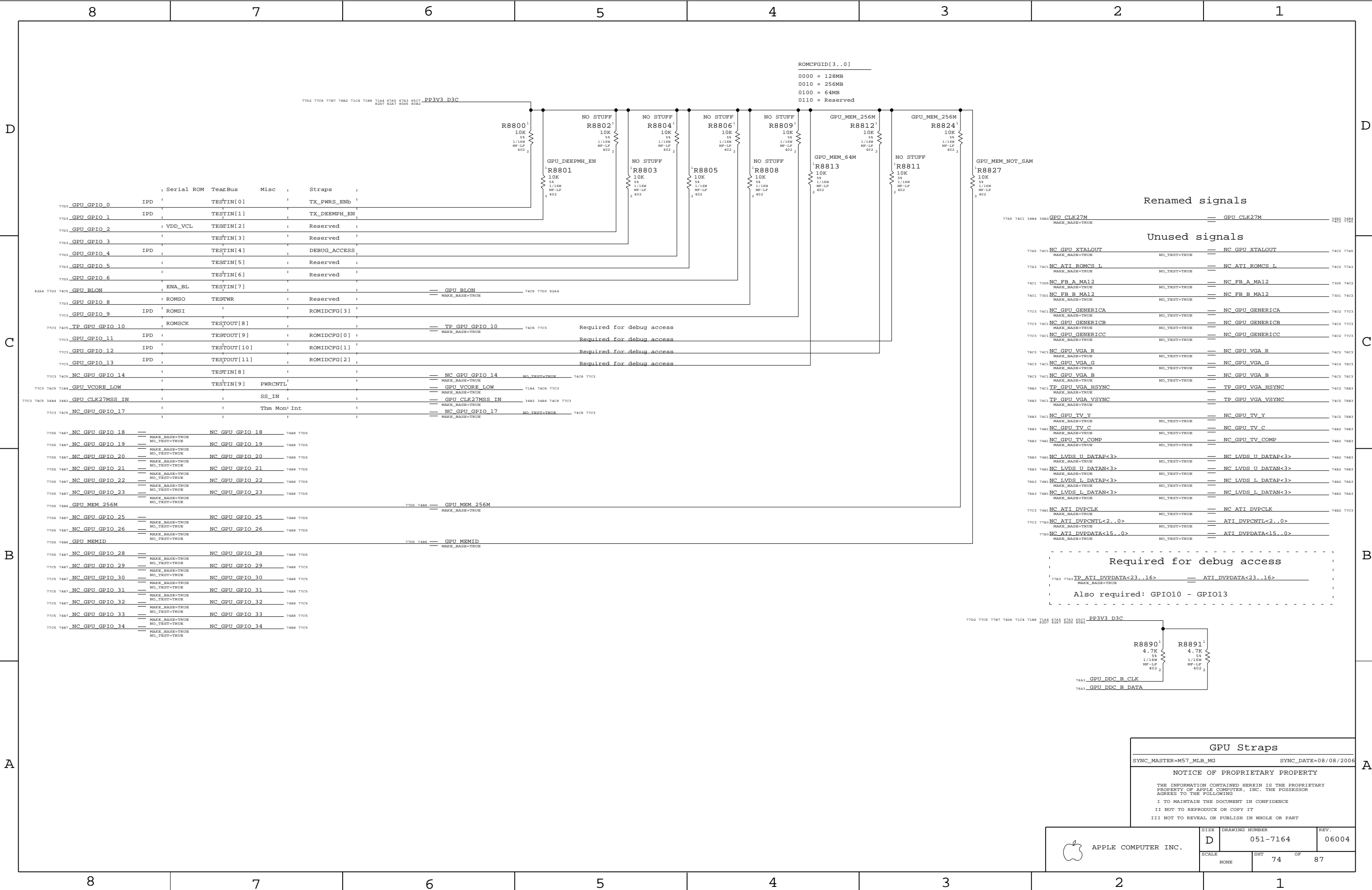
GPU (M56) Core Supplies		
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	D	051-7164	06004
SCALE		SHT	OF
NONE		71	87









Power aliases required by this page:

- =PPIV8\_S0\_FB\_VDD  
- =PPIV8\_S0\_FB\_VDDQSignal aliases required by this page:  
(NONE)BOM options provided by this page:  
(NONE)

## GDDR3 Frame Buffer A

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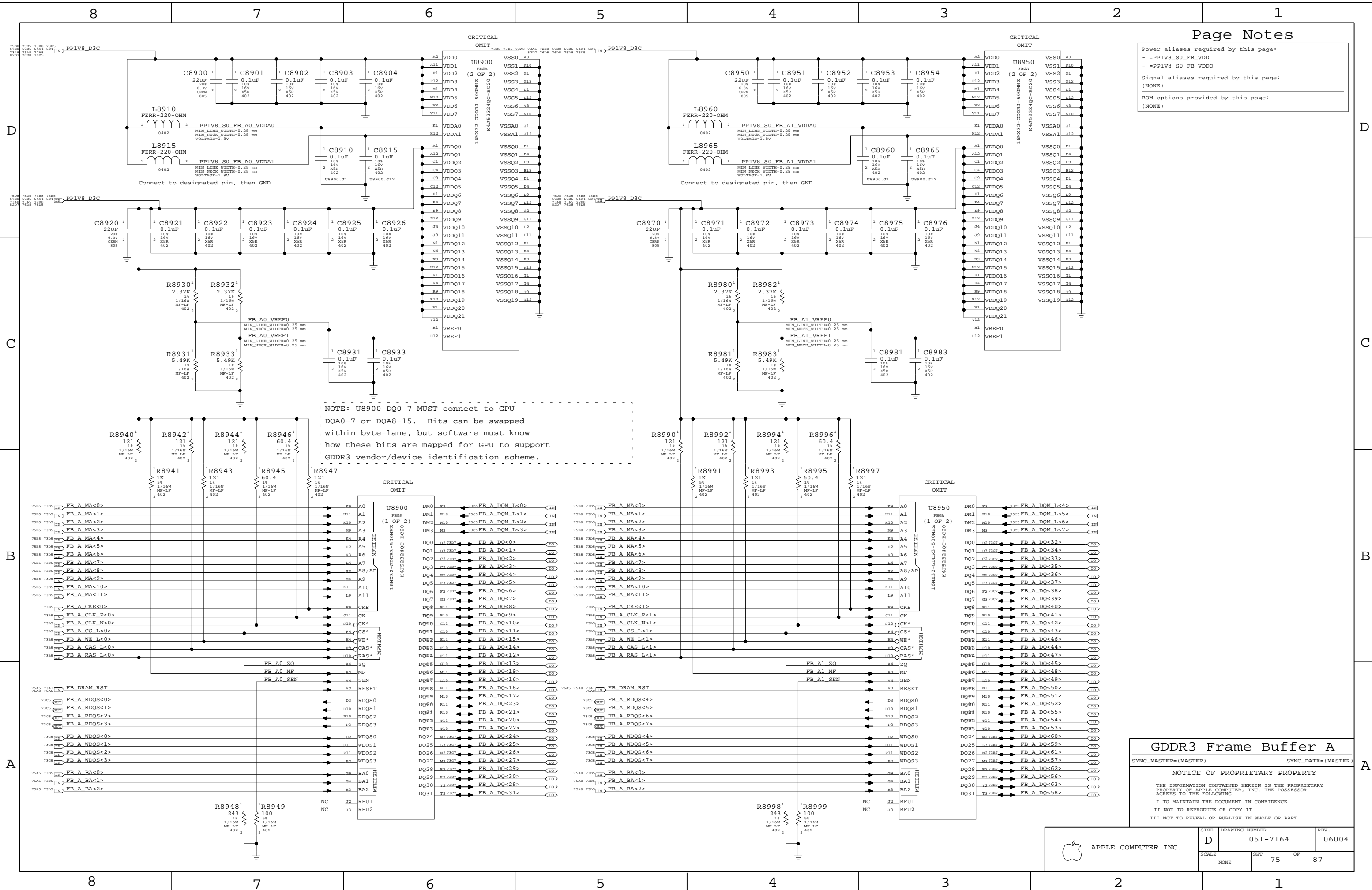
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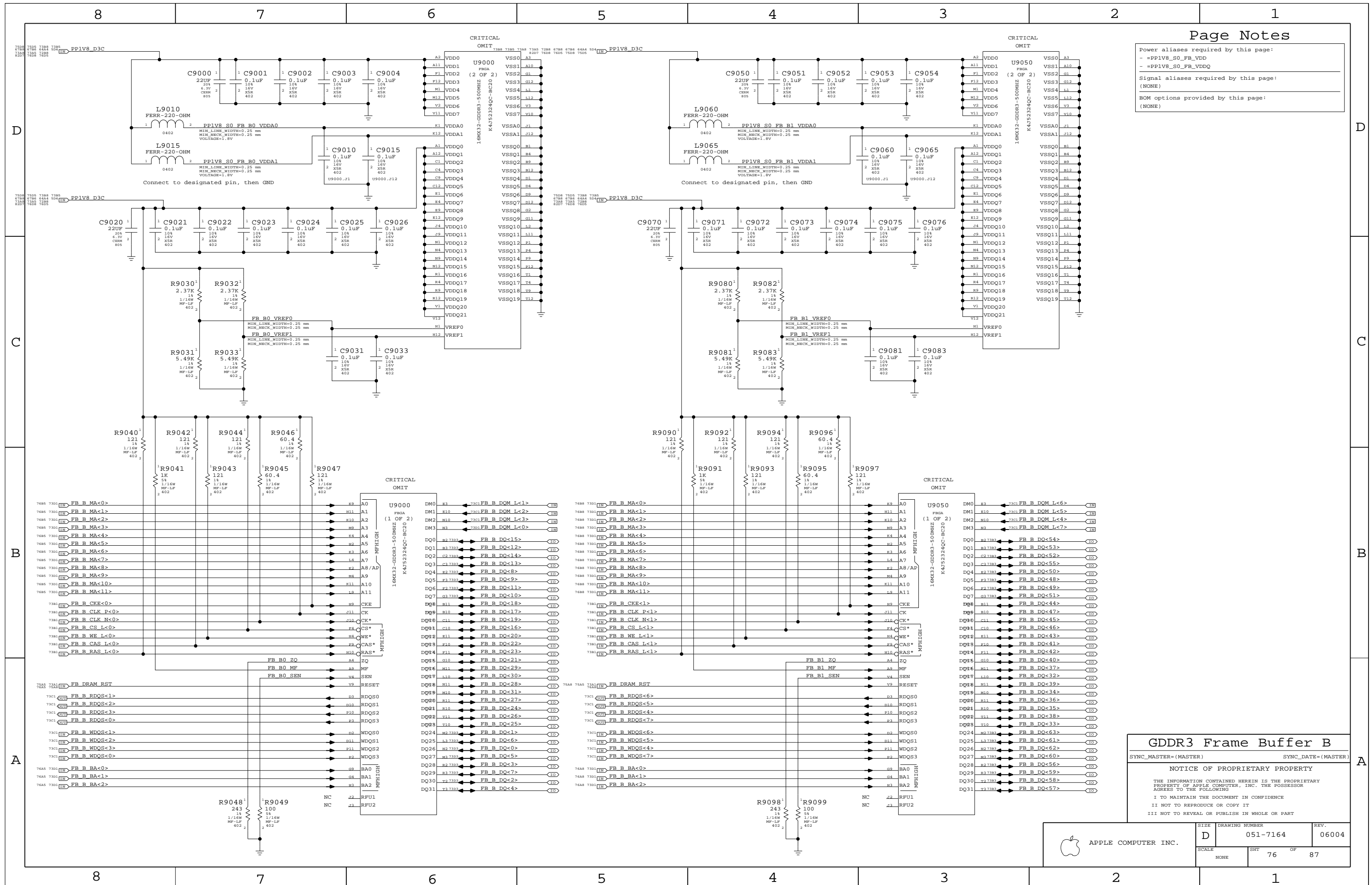
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## Page Notes

Power aliases required by this page:

- =PP3V3\_GPU\_GPIOS  
- =PP2V5\_PVDD  
- =PP1V8\_GPU\_LVDS\_PLL

Signal aliases required by this page:

- =I2C\_GPU\_TMDS\_SDA - I2C data line for external TMDS transmitters  
- =I2C\_GPU\_TMDS\_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:

(NONE)

7488 7487 NC GPU GPIO 18 AE13 GPIO\_18  
7488 7487 NC GPU GPIO 19 AF13 GPIO\_19  
7488 7487 NC GPU GPIO 20 AE9 GPIO\_20  
7488 7487 NC GPU GPIO 21 AG7 GPIO\_21  
7488 7487 NC GPU GPIO 22 AE10 GPIO\_22  
7488 7487 NC GPU GPIO 23 AE9 GPIO\_23  
7488 7486 GPU MEM 256M AE7 GPIO\_24  
7488 7487 NC GPU GPIO 25 AE8 GPIO\_25  
7488 7487 NC GPU GPIO 26 AH6 GPIO\_26  
7488 7486 GPU MEMID AE10 GPIO\_27  
7488 7487 NC GPU GPIO 28 AG10 GPIO\_28  
7488 7487 NC GPU GPIO 29 AH9 GPIO\_29  
7488 7487 NC GPU GPIO 30 AH8 GPIO\_30  
7488 7487 NC GPU GPIO 31 AH8 GPIO\_31  
7488 7487 NC GPU GPIO 32 AG9 GPIO\_32  
7488 7487 NC GPU GPIO 33 AH7 GPIO\_33  
7488 7487 NC GPU GPIO 34 AG8 GPIO\_34

OMIT  
U8400  
M56P  
BGA  
(6 OF 7)

GENERAL PURPOSE I/O

VREFG AC8 ATI VREFG  
GPIO\_0 AD4 GPU GPIO 0 7408  
GPIO\_1 AD2 GPU GPIO 1 7408  
GPIO\_2 AD1 GPU GPIO 2 7408  
GPIO\_3 AD3 GPU GPIO 3 7408  
GPIO\_4 AC1 GPU GPIO 4 7408  
GPIO\_5 AC2 GPU GPIO 5 7408  
GPIO\_6 AC3 GPU GPIO 6 7408  
GPIO\_7\_BLON AB2 GPU BLON 7405 7408 82A4  
GPIO\_8 AC6 GPU GPIO 8 7408  
GPIO\_9 AC5 GPU GPIO 9 7408  
GPIO\_10 AC4 TP GPU GPIO 10 7405 7408  
GPIO\_11 AB3 GPU GPIO 11 7408  
GPIO\_12 AB4 GPU GPIO 12 7408  
GPIO\_13 AB5 GPU GPIO 13 7408  
GPIO\_14 AD5 NC GPU GPIO 14 7405 7408  
GPIO\_15 AB8 GPU VCORE LOW 7184 7405 7408  
GPIO\_16 AB6 GPU CLK27MSS\_IN 3482 3484 7405 7408  
GPIO\_17 AB7 NC GPU GPIO 17 7405 7408

GENERIC AC22 NC GPU GENERICA 7401 7402  
GENERICB AF23 NC GPU GENERICB 7401 7402  
GENERICC AE23 NC GPU GENERICC 7401 7402  
GENERICD AD23 GPU GENERICD 71A7

PANEL DIGON AE11 GPU DIGON 82A4 82B6  
CONTROL VARY\_BL AD12 GPU VARY BL 82A4  
NC0 AB6 NC  
NC\_DVOVMODE\_0 AC4 NC  
NC\_DVOVMODE\_1 AL4 NC

DVPCLK AG1 NC ATI DVPCLK 7481 7482  
DVPNTL\_0 AF2 NC ATI DVPNTL<0> 7482  
DVPNTL\_1 AE1 NC ATI DVPNTL<1> 7482  
DVPNTL\_2 AF3 NC ATI DVPNTL<2> 7482  
DVPDATA\_0 AG2 NC ATI DVPDATA<0> 7482  
DVPDATA\_1 AG3 NC ATI DVPDATA<1> 7482  
DVPDATA\_2 AB2 NC ATI DVPDATA<2> 7482  
DVPDATA\_3 AB3 NC ATI DVPDATA<3> 7482  
DVPDATA\_4 AB2 NC ATI DVPDATA<4> 7482  
DVPDATA\_5 A11 NC ATI DVPDATA<5> 7482  
DVPDATA\_6 AE2 NC ATI DVPDATA<6> 7482  
DVPDATA\_7 AE1 NC ATI DVPDATA<7> 7482  
DVPDATA\_8 AE3 NC ATI DVPDATA<8> 7482  
DVPDATA\_9 AE2 NC ATI DVPDATA<9> 7482  
DVPDATA\_10 AB3 NC ATI DVPDATA<10> 7482  
DVPDATA\_11 AB3 NC ATI DVPDATA<11> 7482

DVPDATA\_12 AE6 NC ATI DVPDATA<12> 7482  
DVPDATA\_13 AE4 NC ATI DVPDATA<13> 7482  
DVPDATA\_14 AE5 NC ATI DVPDATA<14> 7482  
DVPDATA\_15 AG4 NC ATI DVPDATA<15> 7482  
DVPDATA\_16 AB3 TP ATI DVPDATA<16> 7482  
DVPDATA\_17 AB4 TP ATI DVPDATA<17> 7482  
DVPDATA\_18 AB4 TP ATI DVPDATA<18> 7482  
DVPDATA\_19 AG5 TP ATI DVPDATA<19> 7482  
DVPDATA\_20 AB5 TP ATI DVPDATA<20> 7482  
DVPDATA\_21 AE6 TP ATI DVPDATA<21> 7482  
DVPDATA\_22 AE7 TP ATI DVPDATA<22> 7482  
DVPDATA\_23 AG6 TP ATI DVPDATA<23> 7482

VIP HOST / EXTERNAL TMDS

PLL &amp; XTAL

THERMAL DPLUS AG12 ATI TDIODE P 5486  
DIODE DMINUS AH12 ATI TDIODE N 5486  
ROM ROMCS\* AC7 NC ATI ROMCS L 7401 7402  
TEST TESTEN AG22 ATI TESTEN

7706 7787 7406 7482 7104 7188 71A4 67A5 67A3 65C7 PP3V3 D3C  
8207 82A7 80D5 80B2

Typically <50mA  
C9100 22UF 20A 6.3V CERM 805  
C9101 1uF 10A 6.3V CERM 402  
C9102 1uF 10A 6.3V CERM 402  
C9103 1uF 10A 6.3V CERM 402

8207 78C8 7706 77A8 67A8 67A6 63C1 5D4 PP2V5 D3C

70mA total for VDD25  
C9110 22UF 20A 6.3V CERM 805  
C9111 1uF 10A 6.3V CERM 402  
C9112 0.1uF 10A 16V XSR 402

8207 78C8 7706 77A8 67A8 67A6 63C1 5D4 PP2V5 D3C

C9115 22UF 20A 6.3V CERM 805  
C9116 1uF 10A 6.3V CERM 402  
C9117 1uF 10A 6.3V CERM 402

7706 7787 7406 7482 7104 7188 71A4 67A5 67A3 65C7 PP3V3 D3C  
8207 82A7 80D5 80B2 77D2

L9120 FERR-220-OHM  
Typically <50mA  
PP1V8R3V3\_S0\_GPU\_VDDR4\_F  
MIN\_LINE\_WIDTH=0.25 mm  
MIN\_NECK\_WIDTH=0.25 mm  
VOLTAGE=3.3V

C9120 22UF 20A 6.3V CERM 805  
C9121 1uF 10A 6.3V CERM 402  
C9122 0.1uF 10A 16V XSR 402

7706 7787 7406 7482 7104 7188 71A4 67A5 67A3 65C7 PP3V3 D3C  
8207 82A7 80D5 80B2 77D2

L9125 FERR-220-OHM  
Typically <50mA  
PP1V8R3V3\_S0\_GPU\_VDDR5\_F  
MIN\_LINE\_WIDTH=0.25 mm  
MIN\_NECK\_WIDTH=0.25 mm  
VOLTAGE=3.3V

C9125 22UF 20A 6.3V CERM 805  
C9126 1uF 10A 6.3V CERM 402  
C9127 0.1uF 10A 16V XSR 402

8207 78C7 70A1 67D8 67D6 67C6 63B1 5D4 PP1V2 D3C

L9130 200-OHM-EMI  
PP1V2\_S0\_GPU\_VDDPLL  
MIN\_LINE\_WIDTH=0.25 mm  
MIN\_NECK\_WIDTH=0.2 mm  
VOLTAGE=1.2V

C9130 22UF 20A 6.3V CERM 805  
C9131 1uF 10A 6.3V CERM 402  
C9132 1uF 10A 6.3V CERM 402

(PP2V5\_S0\_GPU\_PVDD\_F)  
(PP1V0R1V2\_S0\_GPU\_MPVD)

8207 78C8 7706 67A8 67A6 63C1 5D4 PP2V5 D3C

L9135 FERR-220-OHM  
PP2V5\_S0\_GPU\_PVDD\_F  
MIN\_LINE\_WIDTH=0.25 mm  
MIN\_NECK\_WIDTH=0.25 mm  
VOLTAGE=2.5V

C9135 22UF 20A 6.3V CERM 805  
C9136 1uF 10A 6.3V CERM 402  
C9137 0.1uF 10A 16V XSR 402

74C1 3484 3482 GPU\_CLK27M  
74C2 74C1 NC GPU XTALOUT

72D8 71C1 71B7 67A8 67A6 55C7 55A5 5B3 PPVCORE D3C GPU

L9140 FERR-220-OHM  
PPVCORE\_S0\_GPU\_MPVD  
MIN\_LINE\_WIDTH=0.2 mm  
MIN\_NECK\_WIDTH=0.2 mm  
VOLTAGE=1.2V

C9140 22UF 20A 6.3V CERM 805  
C9141 1uF 10A 6.3V CERM 402  
C9142 0.1uF 10A 16V XSR 402



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## ATI M56 GPIO/DVO/Misc

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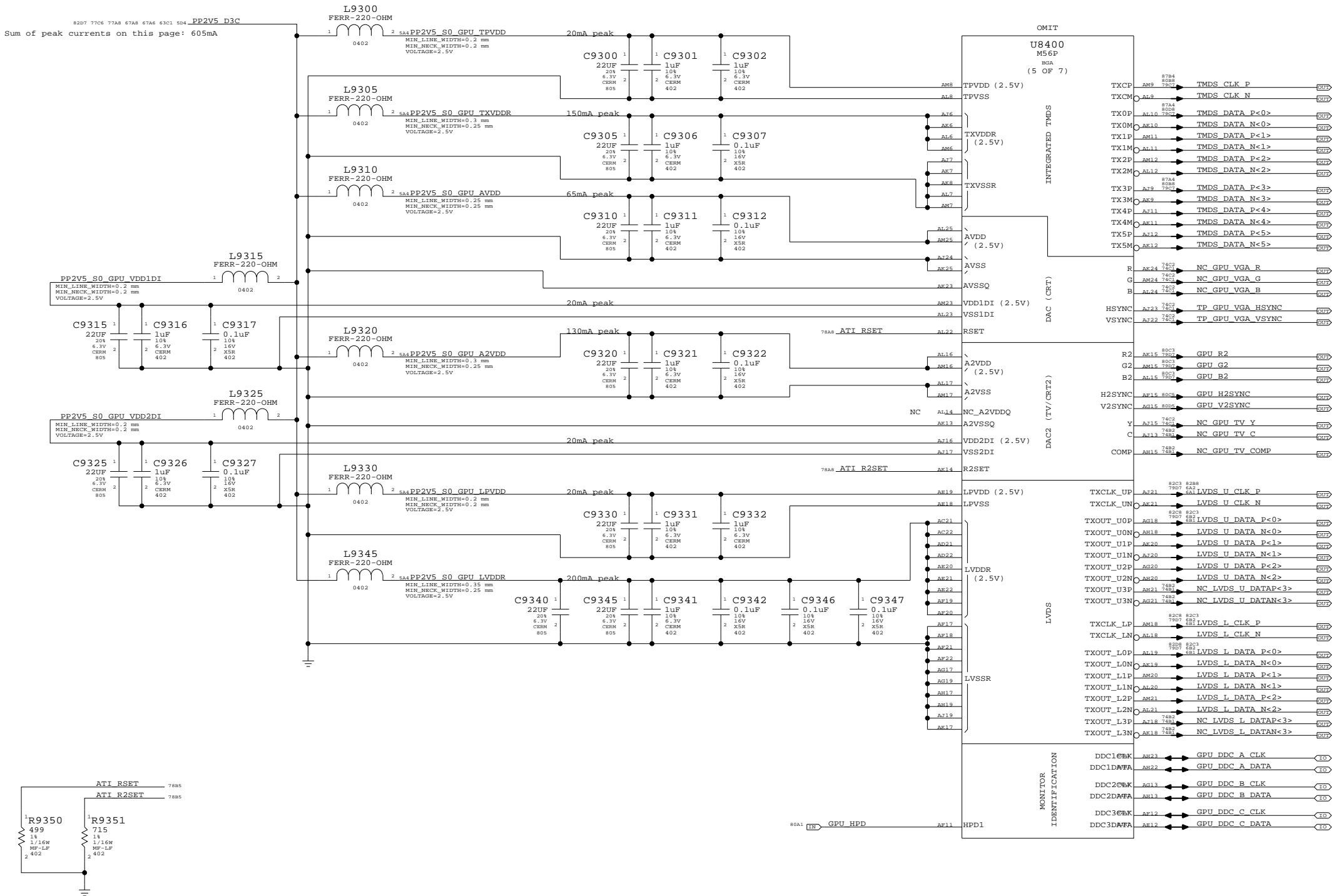
- =PP2V5\_S0\_GPU  
- =PP1V8R2V5\_S0\_GPU\_LVDDR

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



## ATI M56 Video Interfaces

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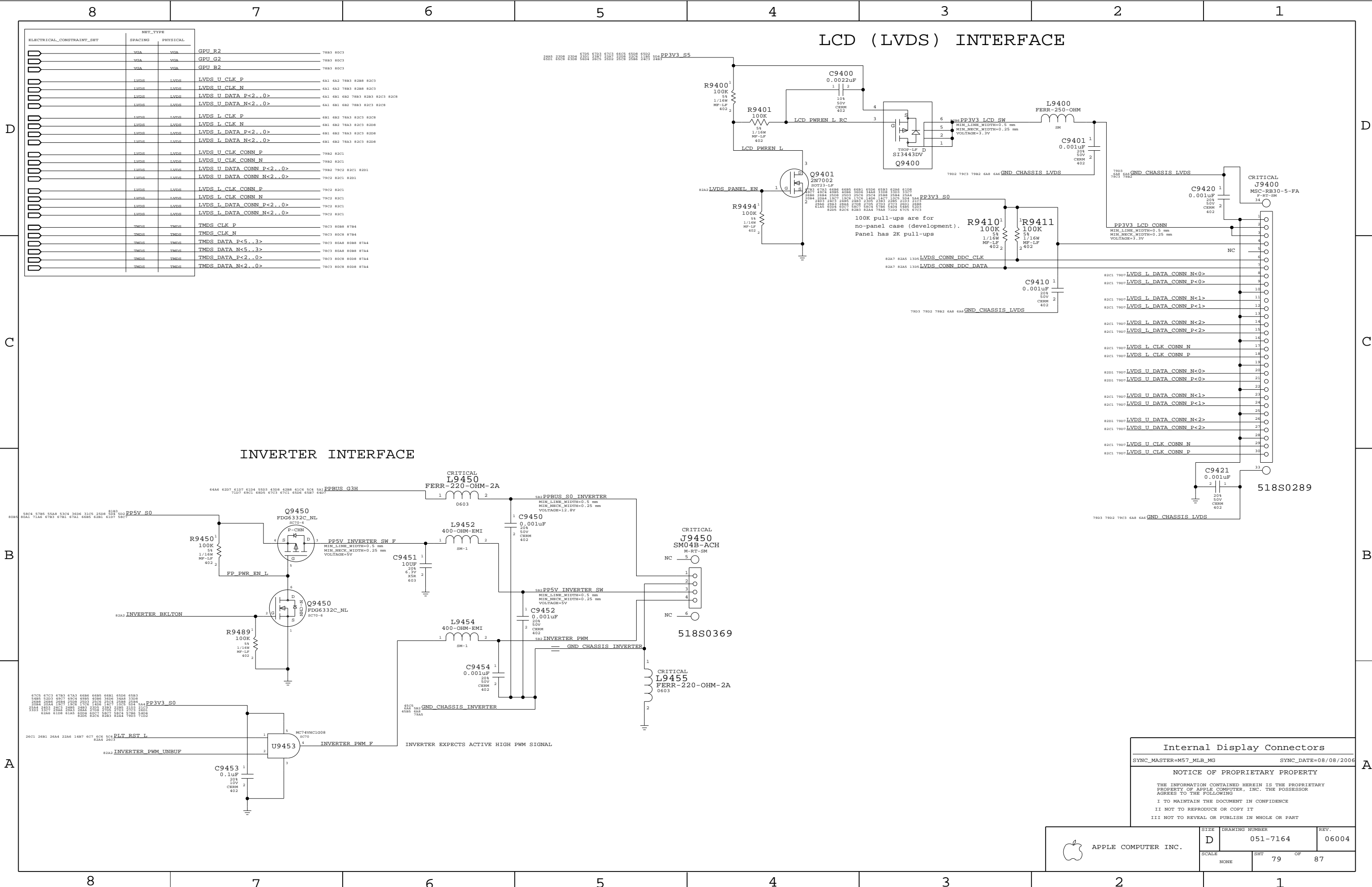
NONE

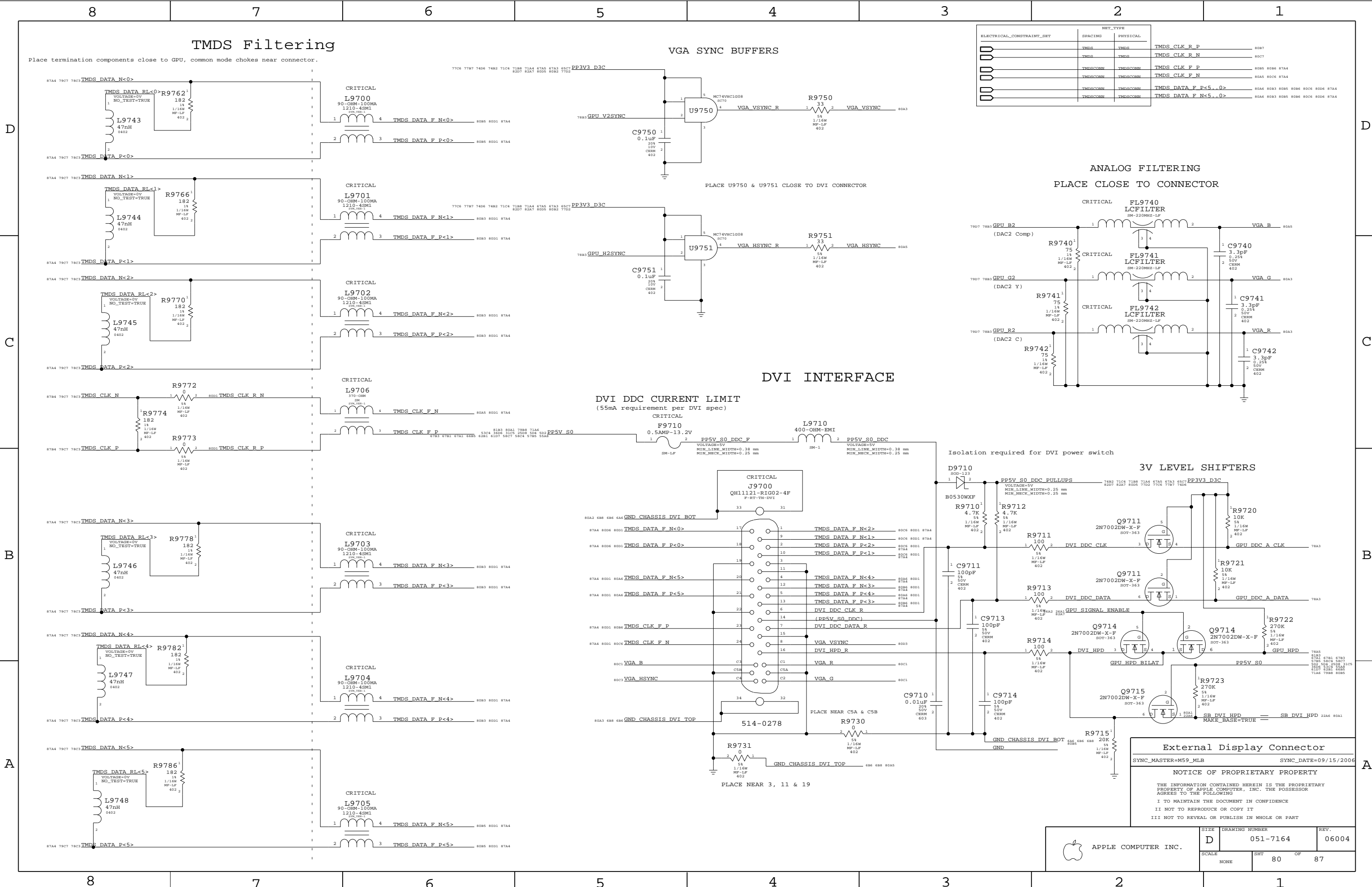
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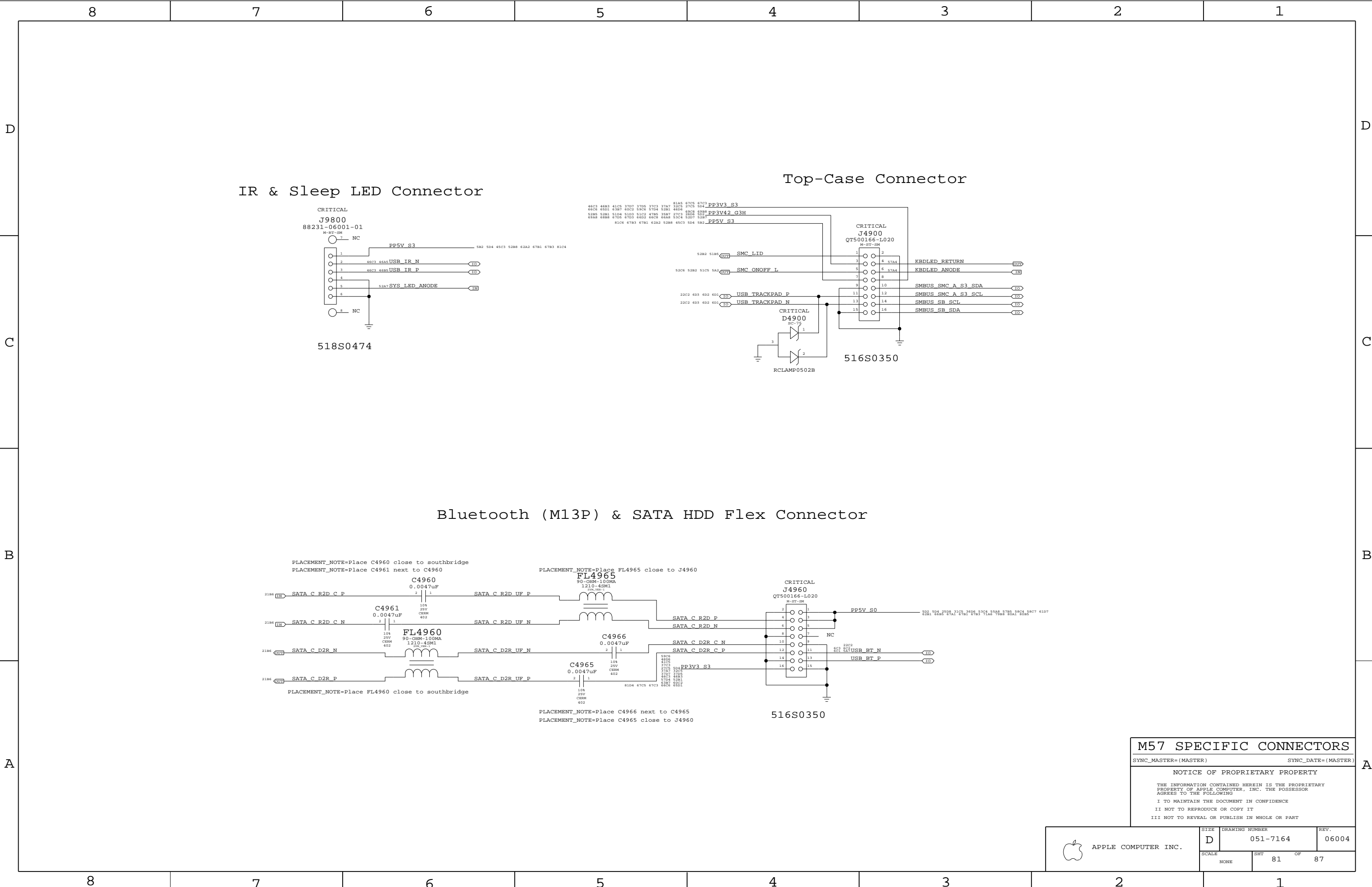
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M57 SPECIFIC CONNECTORS

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## LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.

## PGOOD Monitor for GPU Rails

D3CPGOOD\_ALL BOM option stuffs LTC2903 circuit to monitor all D3C rails to qualify D3CPGOOD.  
D3CPGOOD\_3V3 BOM option uses only PP3V3\_D3C to qualify D3CPGOOD.

## LVDS I/F Mux

### NB LVDS I/F

### GPU LVDS I/F

## Panel/Backlight Control Mux

## GPU DDC Pass FETs

### LVDS Interface Pull-downs

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<div>Revision History</div>															
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C															
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Revision History

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GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_3S_TO_5S	*	Y	=35_OHM_SE	=55_OHM_SE	=35_55_OHM_SE	=STANDARD	=STANDARD
FB_40S	*	Y	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
FB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FB_ADCTRL	*	=2.5:1_SPACING	?
FB_CLK	*	=2.5:1_SPACING	?
FB_DATA	*	=2.5:1_SPACING	?

ADDR/Ctrl lines should route 35-ohms to T, then 55-ohms to each VRAM device.  
Ctrl lines are 55-ohm single-ended impedance.  
DQ/DQM/QoS lines are 40-ohm single-ended impedance.

Note: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.  
Note: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"  
Source: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADeON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_Set	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_Ohm_DIFF	=100_Ohm_Diff	=100_Ohm_Diff	=100_Ohm_Diff	=100_Ohm_Diff
TMDs_100D	*	Y	=100_Ohm_Diff	=100_Ohm_Diff	=100_Ohm_Diff	=100_Ohm_Diff	=100_Ohm_Diff
VGA_75S	*	Y	=75_Ohm_Se	=75_Ohm_Se	=75_Ohm_Se	=STANDARD	=STANDARD

SPACING_RULE_Set	LAYER	Line-to-Line Spacing	Weight
LVDS	*	=3:1_SpAcIng	?
TMDs	*	=3:1_SpAcIng	?
vGa	*	15 MIL	?

Net_SpAcInG_TyPe1	Net_SpAcInG_TyPe2	Area_Type	SpacinG_Rule_Set
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDs	TMDs	*	TMDs_PAIR2PAIR

LVDS and TMds signals are 100-ohm +/- 10% differential impedance.  
LVDS and TMds pairs should be kept at least 25 mils apart.  
Ground shields can be used around each pair if spacing cannot be met.  
VGA should be routed as close to 75-ohms single-ended impedance as possible.  
vGa signals should be kept at least 15 mils from other traces.  
Ground shields recommended around vGa signals.

Note: Layout Guide does not specify LVDS/TMds spacing to other traces other than "do not run close"

Source: ATi Layout Guide, Rev 0.5 (DSG-216MOBRADeON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_Set	LAYER	ALLOW ROUTE ON LAYER?	MinImUm LinE Width	MInIMUM Neck width	MAxI MuM neck Length	dIfFfPaIr PRIMAry GAp	dIfFfPaIr NeCk GAp
eNeT_100D	*	y	=100_Ohm_Diff	=100_Ohm_Diff	=100_Ohm_Diff	=100_Ohm_Diff	=100_Ohm_Diff
Pw_110D	*	y	=110_Ohm_Diff	=110_Ohm_Diff	=110_Ohm_Diff	=110_Ohm_Diff	=110_Ohm_Diff

SpAcInG_Rule_Set	LAYER	LinE-tO-lINe SpACIng	WeIGht
EneT	*	=3:1_SpAcIng	?
PW	*	=3:1_SpAcIng	?

note

PCI Bus Constraints

Physical_rule_set	Layer	Allow Route On Layer?	Minimum Line Width	Minimum Neck Width	Maximum Neck Length	Diffpair Primary Gap	Diffpair Neck Gap
pCI_55S	*	y	=55_Ohm_Se	=55_Ohm_Se	=55_Ohm_Se	=STANDARD	=STANDARD

Spacing_Rule_Set	Layer	Line-To-Line Spacing	Weight
pCi	*	=2:1_SpAcIng	?

More System Constraints

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DRAWING NUMBER 051-7164

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M9 Board-Specific Spacing & Physical Constraints															
BOARD LAYERS								BOARD AREAS				BOARD UNITS (MIL OR MM)		ALLEGRO VERSION	
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM								NO_TYPE, BGA				MM		15.2	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
DEFAULT		*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM							
STANDARD		*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
55_OHM_SE		TOP, BOTTOM	Y	0.100 MM	0.100 MM										
55_OHM_SE		*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
50_OHM_SE		TOP, BOTTOM	Y	0.124 MM	0.124 MM										
50_OHM_SE		*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
45_OHM_SE		TOP, BOTTOM	Y	0.150 MM	0.150 MM										
45_OHM_SE		*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
40_OHM_SE		TOP, BOTTOM	Y	0.185 MM	0.185 MM										
40_OHM_SE		*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
35_OHM_SE		TOP, BOTTOM	Y	0.230 MM	0.230 MM										
35_OHM_SE		*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
27P4_OHM_SE		TOP, BOTTOM	Y	0.335 MM	0.335 MM										
27P4_OHM_SE		*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
35_55_OHM_SE		TOP, BOTTOM	Y	0.230 MM	0.100 MM										
35_55_OHM_SE		*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD							
Unsupported rule															
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
75_OHM_SE		*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
70_OHM_DIFF		*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM							
70_OHM_DIFF		TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
75_OHM_DIFF		*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM							
75_OHM_DIFF		TOP, BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
80_OHM_DIFF		*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM							
80_OHM_DIFF		TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
85_OHM_DIFF		*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM							
85_OHM_DIFF		TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
90_OHM_DIFF		*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM							
90_OHM_DIFF		TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
100_OHM_DIFF		*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM							
100_OHM_DIFF		TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM							
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
110_OHM_DIFF		*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM							
110_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM							

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2, ISL11	0.1 MM	?
1.8:1_SPACING	ISL2, ISL11	0.1 MM	?
2:1_SPACING	ISL2, ISL11	0.1 MM	?
2.5:1_SPACING	ISL2, ISL11	0.1 MM	?
3:1_SPACING	ISL2, ISL11	0.1 MM	?
4:1_SPACING	ISL2, ISL11	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2, ISL11	0.1 MM	?
CLK_PCIE	ISL2, ISL11	0.1 MM	?
CLK_MED	ISL2, ISL11	0.1 MM	?
CLK_SLOW	ISL2, ISL11	0.1 MM	?
CPU_COMP	ISL2, ISL11	0.1 MM	?
CPU_GTLREF	ISL2, ISL11	0.1 MM	?
CPU_VCCSENSE	ISL2, ISL11	0.1 MM	?
DMI	ISL2, ISL11	0.1 MM	?
LVDS_PAIR2PAIR	ISL2, ISL11	0.1 MM	?
MEM_2OTHER	ISL2, ISL11	0.1 MM	?
PCIE	ISL2, ISL11	0.1 MM	?
SATA	ISL2, ISL11	0.1 MM	?
TMDS_PAIR2PAIR	ISL2, ISL11	0.1 MM	?
VGA	ISL2, ISL11	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI OVERRIDE	* OVERRIDE	0.1 MM OVERRIDE	? OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE

M9 Spacing & Physical Constraints															
SYNC_MASTER=(MASTER)								SYNC_DATE=(MASTER)							
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